REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline Y. Correction to t_{LZ} in Table IA. Corrections to t_{AC} header lines in timing diagrams. - glg	13-03-26	Charles Saffle

REV	A	A	A	A	A	A														
SHEET	55	56	57	58	59	60														
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS																			
REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A

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DRAWING APPROVAL DATE
12-09-06

REVISION LEVEL
A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY All DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 16-MEG X 48-BIT X 4-BANK (3-GIG), RADIATION-HARDENED, SYNCHRONOUS DRAM (SDRAM), MULTICHIP MODULE

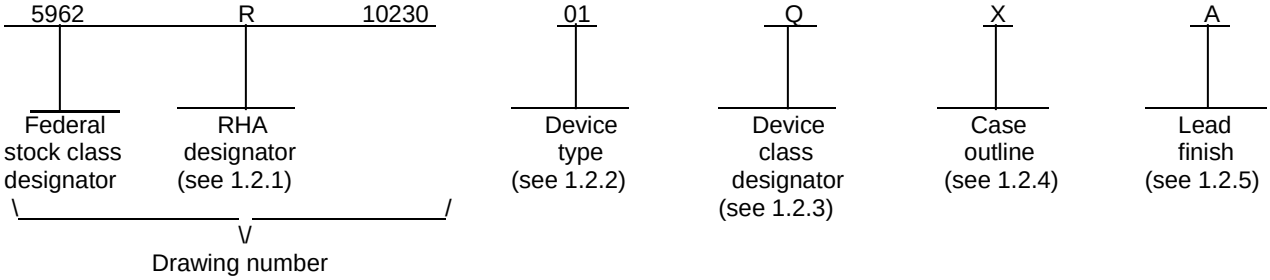
SIZE	CAGE CODE	
A	**67268**	**5962-10230**

SHEET 1 OF 60

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	8SDMQ64M48	16M X 48-bit X 4-bank SDRAM	7.5 ns
02	8SDMQ64M48	16M X 48-bit X 4-bank SDRAM, with additional screening 1/	7.5 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	128	dual cavity quad flat pack
Y	See figure 1	128	dual cavity quad flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38535 for classes Q and V.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range, (V_{DD},V_{DDQ})	-1.0 V dc to +4.3 V dc
Voltage range on any pin relative to ground	-0.3 V dc to V_{DD} +0.3 V dc
Power dissipation permitted, P_D @ T_C = 105ºC	4.0 W
Storage temperature range, (T_{STG})	-65ºC to +150ºC
Junction temperature, (T_J)	+125ºC
Thermal resistance, junction-to-case, (θ_{JC}): Case X	5ºC/W

1.4 Recommended operating conditions.

Positive supply voltage, (V_{DD},V_{DDQ})	+3.0 V dc to +3.6 V dc
Input voltage, dc	0 V dc to V_{DDQ}
Case operating temperature range, (T_C)	-40ºC to +105ºC

1/ Device type 02 provides QML Q product with additional testing as specified in paragraph 4.2.1d.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltage values in this drawing are with respect to V_{SS}.

1.5 Radiation features

Maximum total dose available (dose rate = 50 - 300 rads(Si)/s)..... 100 krads(Si) 5/
Single event phenomenon (SEP):
No SEU occurs at effective LET (see 4.4.4.2)..... < 0.8 MeV-cm^2/mg 6/
No SEL occurs at effective LET (see 4.4.4.2) ..... ≤ 111 MeV-cm^2/mg
(SEU event rate = 1.3 x 10^{-10} events/bit-day with cross section 7.6 x 10^{-10} cm^2/bit).

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC INTERNATIONAL (JEDEC)

JEDEC Standard Number 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

5/ Device is irradiated in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified herein.

6/ Assuming geosynchronous orbit and Adam's 90% worst environment (based on Space Radiation 5.0).

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Output load circuit. The output load circuit shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.2.6 Radiation test circuit. The radiation test circuit shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request.

3.2.7 Functional tests. Various functional tests used to test this device are contained herein. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in Table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ 2/ $-40°C \le T_C \le +105°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ Unless otherwise specified all voltages referenced to V_{SS}		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High-level input voltage 3/ 4/	V_{IH}			1,2,3	All	2.2		V
Low-level input voltage 3/ 4/	V_{IL}			1,2,3	All		0.6	V
High-level output voltage 3/ 4/	V_{OH}	I_{OH} = -4 mA		1,2,3	All	2.4		V
Low-level output voltage 3/ 4/	V_{OL}	I_{OL} = 4 mA		1,2,3	All		0.4	V
Input capacitance 5/	C_{IN}	f = 1 MHz @ 0 V see 4.4.1e		4	All		75	pF
Bidirectional I/O capacitance 5/	C_{IO}			4	All		25	pF
Input leakage current 3/ 4/	I_{IN}	$0\ V \le V_{IN} \le = V_{DD}$		1,2,3	All	-5	5	µA
Output leakage current 3/ 4/	I_{OZ}	$0\ V \le V_{OUT} \le = V_{DDQ}$ DQs are disabled		1,2,3	All	-5	5	µA
Operating current, active mode 3/ 4/ 6/ 7/ 8/ 9/ 10/ 11/	I_{DD1}	CK = 100 MHz, Burst = 2, READ or WRITE, $t_{RC} = t_{RC}$ (min)		1,2,3	All		450	mA
Standby current, power-down mode 3/ 4/ 7/ 8/ 11/	I_{DD2}	CK = 100 MHz, CKE = LOW, All banks idle		1,2,3	All		15	mA
Standby current, active mode 3/ 4/ 6/ 7/ 8/ 10/ 11/ 12/	I_{DD3}	CK = 100 MHz, $\overline{CS}$ = HIGH, CKE = HIGH, All banks active after t_{RCD} met, No accesses in progress		1,2,3	All		165	mA
Operating current: Burst mode , Page burst 3/ 4/ 6/ 7/ 8/ 9/ 10/ 11/	I_{DD4}	READ or WRITE, All banks active		1,2,3	All		450	mA
Auto refresh current 3/ 4/ 6/ 7/ 8/ 9/ 10/ 11/ 13/	I_{DD5}	$\overline{CS}$ = HIGH, CKE = HIGH	$t_{RFC} = t_{RFC}$ (min)	1,2,3	All		1150	mA
	I_{DD6}		t_{RC} = 3.9 µs	1,2,3	All		150	mA
Functional test		See 4.4.1c, T_C = 25°C		7, 8A, 8B	All			
AC Characteristics 3/ 4/ 7/ 14/ 15/ 16/								
Access time from CLK	$t_{AC(3)}$	See figures 4 and 5 as applicable, Positive edge (CL = 3)		9,10,11	All		7.5	ns
Access time from CLK	$t_{AC(2)}$	See figures 4 and 5 as applicable, Positive edge (CL = 2)		9,10,11	All		7.5	ns
Address hold time	t_{AH}	See figures 4 and 5 as applicable		9,10,11	All	1.5		ns
Address setup time	t_{AS}			9,10,11	All	1.5		ns
CLK, high-level width	t_{CH}			9,10,11	All	4		ns
CLK, low-level width	t_{CL}			9,10,11	All	4		ns
Clock cycle time, CL = 3 17/	t_{CK3}			9,10,11	All	10		ns
Clock cycle time, CL = 2 17/	t_{CK2}			9,10,11	All	10		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-40°C \le T_C \le +105°C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ Unless otherwise specified all voltages referenced to V_{SS}	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Characteristics 3/ 4/ 7/ 14/ 15/ 16/ - continued.							
CKE hold time	t_{CKH}	See figures 4 and 5 as applicable	9,10,11	All	2		ns
CKE setup time	t_{CKS}		9,10,11	All	1.5		ns
$\overline{CS}$ hold time	t_{CMH}		9,10,11	All	2		ns
$\overline{RS}$, $\overline{CAS}$, $\overline{WE}$, hold time			9,10,11	All	1.5		ns
DQM hold time			9,10,11	All	2.5		ns
$\overline{CS}$ setup time	t_{CMS}		9,10,11	All	2.5		ns
$\overline{RS}$, $\overline{CAS}$, $\overline{WE}$, setup time			9,10,11	All	1.5		ns
DQM setup time			9,10,11	All	1.5		ns
Data in hold time	t_{DH}		9,10,11	All	2.5		ns
Data in setup time	t_{DS}		9,10,11	All	1.5		ns
Data out High-Z time, CL = 3	t_{HZ3}		9,10,11	All		9	ns
Data out High-Z time, CL = 2	t_{HZ2}		9,10,11	All		9	ns
Data out Low-Z time	t_{LZ}		9,10,11	All	1		ns
Data out hold time (load)	t_{OH}		9,10,11	All	2.7		ns
Data out hold time (no load) 18/	t_{OHN}		9,10,11	All	1.8		ns
ACTIVE-to-PRECHARGE command period 18/	t_{RAS}		9,10,11	All	44	60K	ns
ACTIVE-to-ACTIVE command period	t_{RC}		9,10,11	All	66		ns
ACTIVE-to-READ or WRITE delay	t_{RCD}		9,10,11	All		20	ns
Refresh period (8,192 rows) 19/	t_{REF}		9,10,11	All		32	ms
AUTO REFRESH period	t_{RFC}		9,10,11	All	66		ns
PRECHARGE command period	t_{RP}		9,10,11	All	20		ns
Active bank a-to-ACTIVE bank b command	t_{RRD}		9,10,11	All	15		ns
Transition time 14/	t_T		9,10,11	All	0.3	1.2	ns
WRITE recovery time	t_{WR}		9,10,11	All	20		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions 1/ 2/ $-40^{\circ}C \le T_C \le +105^{\circ}C$ $+3.0\ V \le V_{DD} \le +3.6\ V$ Unless otherwise specified all voltages referenced to V_{SS}	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC Functional Characteristics 3/ 4/ 7/ 14/ 20/ 21/							
READ/WRITE command-to-READ/WRITE command	t_{CCD}	See figures 4 and 5 as applicable	9,10,11	All	1		t_{CK}
CKE to clock disable or power-down entry mode	t_{CKED}		9,10,11	All	1		t_{CK}
CKE to clock enable or power-down exit setup mode	t_{PED}		9,10,11	All	1		t_{CK}
DQM input data delay	t_{DQD}		9,10,11	All	0		t_{CK}
DQM to data mask during WRITEs	t_{DQM}		9,10,11	All	0		t_{CK}
DQM to data High-Z during READs	t_{DQZ}		9,10,11	All	2		t_{CK}
WRITE command to input data delay	t_{DWD}		9,10,11	All	0		t_{CK}
Data-in to ACTIVE command	t_{DAL}		9,10,11	All	5		t_{CK}
Data-in to PRECHARGE command	t_{DPL}		9,10,11	All	2		t_{CK}
Last data-in to burst STOP command	t_{BDL}		9,10,11	All	1		t_{CK}
Last data-in to new READ/WRITE command	t_{CDL}		9,10,11	All	1		t_{CK}
Last data-in to PRECHARGE command	t_{RDL}		9,10,11	All	2		t_{CK}
Load mode register command to ACTIVE or REFRESH command	t_{MRD}		9,10,11	All	2		t_{CK}
Data out to High-Z from PRECHARGE command	$t_{ROH(3)}$		9,10,11	All	3		t_{CK}
	$t_{ROH(2)}$		9,10,11	All	2		t_{CK}

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Devices supplied to this drawing meet all levels M, D, P, L, and R of irradiation. However, these devices are only characterized at the "R" level. Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C$

3/ The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($-40^{\circ}C \le T_C \le +105\ ^{\circ}C$) is ensured.

4/ An initial pause of 100 µs is required after power-up followed by two AUTO REFRESH commands, before proper device operation is ensured. V_{DD} and V_{DDQ} must be powered up simultaneously. V_{SS} and V_{SSQ} must be at the same potential. The two AUTO REFRESH command wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.

5/ Measured only for initial qualification and after any design or process change which could affect this parameter.

6/ I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and outputs open.
7/ AC timing and I_{DD} tests are set with timing referenced to a 1.5V crossover point.
8/ I_{DD} specifications are tested after the device is properly initialized.
9/ The I_{DD} current will increase or decrease in a proportional amount by the amount the frequency is altered for the test condition.
10/ Address transitions average one transition every two clocks.
11/ CL = 2, t_{CK} = 10 ns.
12/ Other input signals are allowed to transition no more than once every two clocks and are otherwise valid at V_{IH} or V_{IL} levels.
13/ CKE is HIGH during refresh command period tRFC (Min) else CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value.
14/ AC characteristics assume t_T = 1 ns, supplied as a design limit, neither tested nor guaranteed.
15/ In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16/ Outputs measured at 1.5V with equivalent test load circuit.
17/ The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR}, and PRECHARGE commands) CKE may be used to reduce the data rate.
18/ Guaranteed by design only and not characterized or tested.
19/ Guaranteed by characterization testing.
20/ Functionally tested only.
21/ t_{CK} is one clock cycle but is not a fixed value. The clock periods are variable and depend upon the speed at which the the device is operating. Table IA defines how many clock cycles are required between operations.

Table IB. SEP test limits 1/ 2/

Device type	Single Event Upset 3/ 4/ V_{DD} = 3.0 V		Single Event Latch-up 5/ Biased V_{DD} = 3.6 V
	Effective LET No upsets [MeV/(mg/cm^2)]	Maximum device Cross section (cm^2/bit)	Effective LET No latch-up [MeV/(mg/cm^2)]
All	< 0.8	7.6×10^{-10}	≤ 111

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Test temperature T_A = +25°C ±10°C.
4/ A SEU event rate of 1.3E-10 events/bit-day was calculated for the 90% worst-case environment in the geosynchronous orbit with respect to onset LET 0.8 MeV-cm^2/mg at devices saturated cross section 7.6×10^{-10} cm^2/bit. This event rate can be converted to an event frequency of 14 device-days/event. For details on SEE test contact the device manufacturer.
5/ Worst case test temperature T_A = +105°C ±10°C.

Case outline X

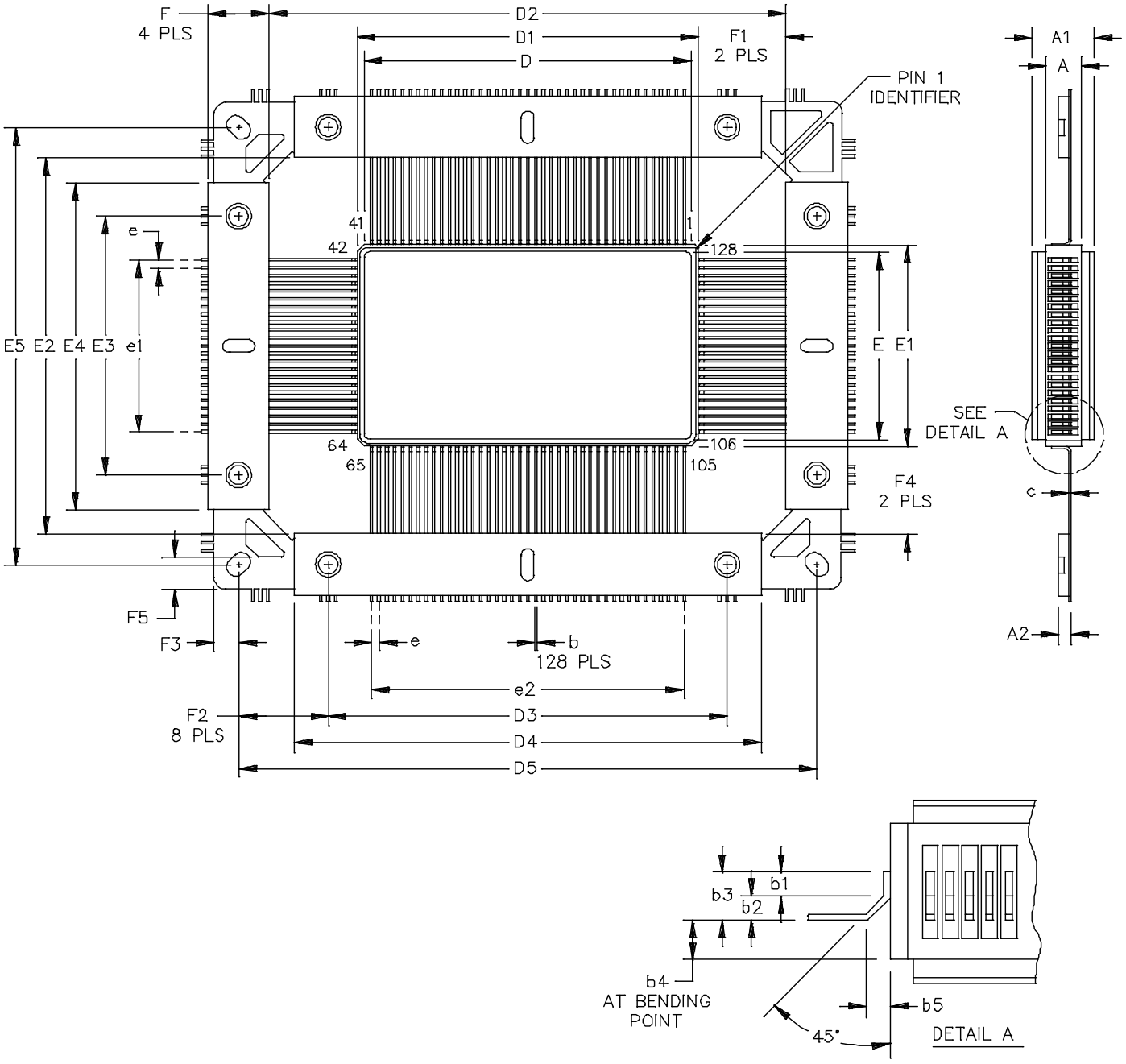


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-10230
DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990		REVISION LEVEL A	SHEET 9

DSCC FORM 2234
APR 97

Case outline X

Symbol	Millimeters	
	Min	Max
A	3.51	4.29
A1		5.65
A2	0.89 (REF)	
b	0.150	0.250
b1	0.86 Max.	
b2	0.70 (REF)	
b3	1.25	1.55
b4	0.75	1.05
b5	0.70 (REF)	
c	0.125	0.200
e	0.635 (REF)	
e1	13.97	
e2	25.40	
D	26.28	26.82
D1	27.49	28.13
D2	42.55 (REF)	
D3	32.64 (REF)	
D4	37.97 (REF)	
D5	47.63 (REF)	
E	14.85	15.15
E1	16.12	16.44
E2	30.43 (REF)	
E3	20.52 (REF)	
E4	25.86 (REF)	
E5	35.51 (REF)	
F	5.08 (REF)	
F1	7.37 (REF)	
F2	7.49 (REF)	
F3	2.03 (REF)	
F4	7.08 (REF)	
F5	2.54 (REF)	

NOTES:
1. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
2. The seal ring and lids are electrically connected to V_{SS}.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Tie bar may have excise slots of various configurations and are vendor option. Tie bar dimensions are for reference only.
5. Package material: opaque 90% minimum Alumina ceramic.
6. ESD classification mark is located in the pin 1 corner.
7. For Detail A, dogleg geometries optional within dimensions shown.

FIGURE 1. Case outline - Continued.

Case outline Y

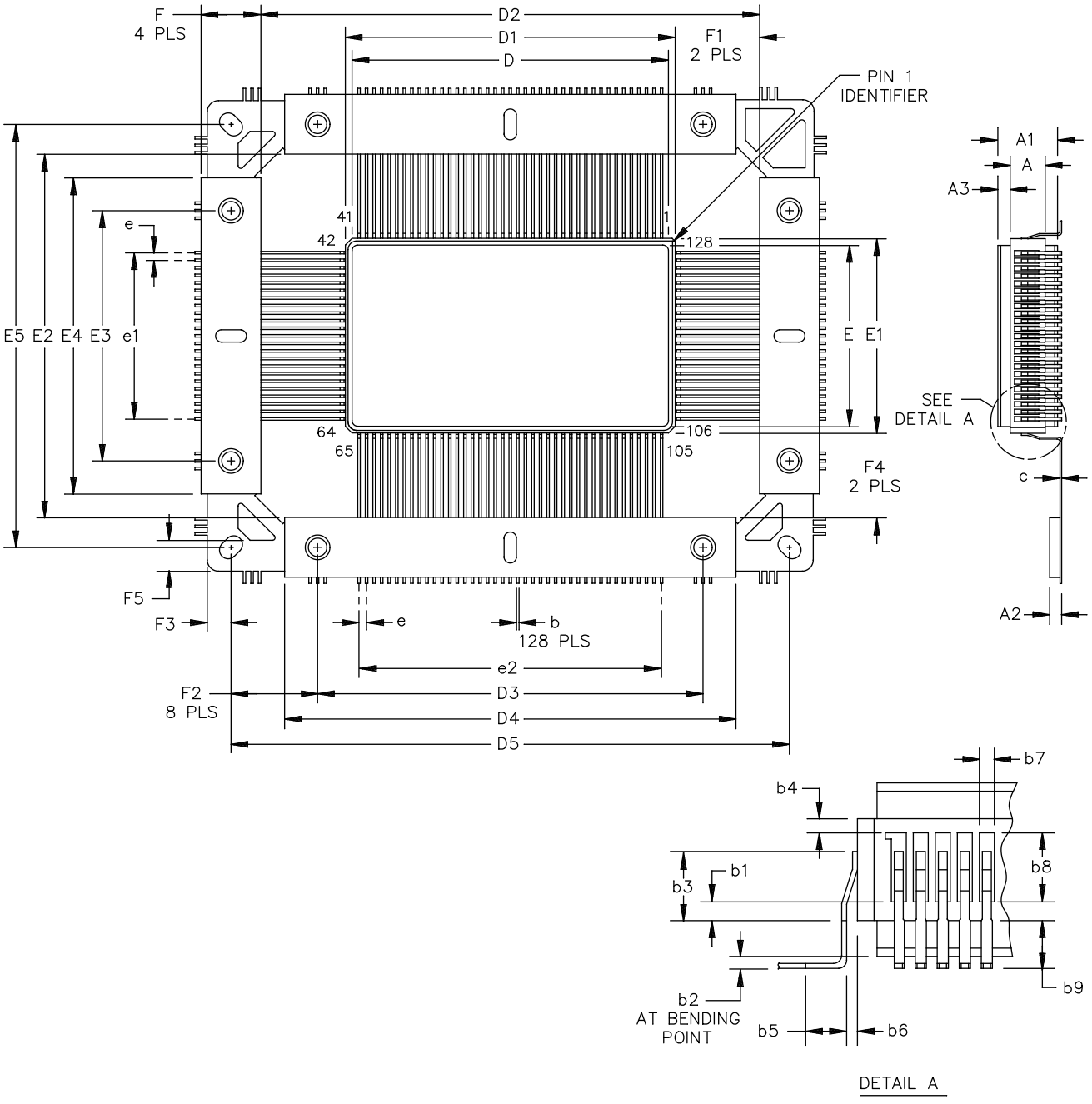


FIGURE 1. Case outline - continued.

Case outline Y

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max.		Min	Max.
A	3.51	4.29	F	5.08 (REF)	
A1		5.65	F1	7.37 (REF)	
A2	0.89 (REF)		F2	7.49 (REF)	
A3	0.63 (REF)		F3	2.03 (REF)	
b	0.30 (REF)		F4	7.075 (REF)	
b1	0.25		F5	2.54 (REF)	
b2	0.13	0.53			
b3	2.148 (REF)				
b4	0.25				
b5	1.00 (REF)				
b6	0.25 (REF)				
b7	0.38	0.54			
b8	2.70 (REF)				
b9	1.00 (REF)				
c	0.125	0.200			
e	0.635 (REF)				
e1	13.97 (REF)				
e2	25.40 (REF)				
D	26.28	26.82			
D1	27.49	28.13			
D2	42.55 (REF)				
D3	32.64 (REF)				
D4	37.97 (REF)				
D5	47.63 (REF)				
E	14.85	15.15			
E1	16.12	16.44			
E2	30.43 (REF)				
E3	20.52 (REF)				
E4	25.86 (REF)				
E5	35.51 (REF)				

NOTES:

1. All exposed metal and metalized areas shall be gold plated per MIL-PRF-38535.
2. The seal ring and lids are electrically connected to V_{SS}.
3. Lead finish is in accordance with MIL-PRF-38535.
4. Tie bar may have excise slots of various configurations and are vendor option. Tie bar dimensions are for reference only.
5. Package material: opaque 90% minimum Alumina ceramic.
6. ESD classification mark is located in the pin 1 corner.
7. For Detail A, dogleg geometries optional within dimensions shown.

FIGURE 1. Case outline - Continued.

Device type	All	Device type	All
Case outlines	X, Y	Case outlines	X, Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VDDQ	33	DQ5(7)
2	VSSQ	34	VDDQ
3	VSS	35	VSSQ
4	VDD	36	VSS
5	VDDQ	37	VDD
6	VSSQ	38	VDDQ
7	VSS	39	VSSQ
8	VDD	40	VSS
9	VDDQ	41	VDD
10	VSSQ	42	DQ7(0)
11	VSS	43	DQ7(1)
12	VDD	44	DQ0(0)
13	VDDQ	45	DQ0(1)
14	VSSQ	46	DQ6(0)
15	VDDQ	47	DQ6(1)
16	DQM3	48	DQ1(0)
17	DQM5	49	DQ1(1)
18	DQ3(3)	50	DQ5(0)
19	DQ3(5)	51	DQ5(1)
20	DQ4(3)	52	DQ2(0)
21	DQ4(5)	53	DQ2(1)
22	DQ2(3)	54	DQ4(0)
23	DQ2(5)	55	DQ4(1)
24	DQ5(3)	56	DQ3(0)
25	DQ5(5)	57	DQ3(1)
26	DQ1(3)	58	DQM(0)
27	DQ1(5)	59	DQM(1)
28	DQ6(3)	60	VDD
29	DQ6(5)	61	VSS
30	DQ0(3)	62	VSSQ
31	DQ0(5)	63	VDDQ
32	DQ7(3)	64	VSSQ

FIGURE 2. Terminal connections.

Device type	All	Device type	All
Case outlines	X, Y	Case outlines	X, Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
65	VSSQ	102	VSS
66	VDDQ	103	VDD
67	VDD	104	VDDQ
68	VSS	105	VSSQ
69	VSSQ	106	VSS
70	VDDQ	107	VDD
71	VDD	108	VDDQ
72	VSS	109	VSSQ
73	VSSQ	110	NC
74	VDDQ	111	DQM2
75	$\overline{WE}$	112	DQM4
76	$\overline{CAS}$	113	DQ3(2)
77	CLK	114	DQ3(4)
78	$\overline{RAS}$	115	DQ4(2)
79	CKE	116	DQ4(4)
80	$\overline{CS}$	117	DQ2(2)
81	A12	118	DQ2(4)
82	BA0	119	DQ5(2)
83	A11	120	DQ5(4)
84	BA1	121	DQ1(2)
85	A9	122	DQ1(4)
86	A10/AP	123	DQ6(2)
87	A8	124	DQ6(4)
88	A0	125	DQ0(2)
89	A7	126	DQ0(4)
90	A1	127	DQ7(2)
91	A6	128	DQ7(4)
92	A2		
93	A5		
94	A3		
95	A4		
96	VDDQ		
97	VSSQ		
98	VSS		
99	VDD		
100	VDDQ		
101	VSSQ		

FIGURE 2. Terminal connections – Continued.

Commands and DQM Operation Truth Table – 1/, 2/

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	Address	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3/
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H 8/	Bank/Col	X	4/
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H 8/	Bank/Col	Valid	4/
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5/
AUTO REFRESH	L	L	L	H	X	X	X	6/, 7/
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	4/
Write enable/output enable	--	--	--	--	L	--	Active	8/
Write inhibit/output High-Z	--	--	--	--	H	--	High-Z	8/

1. CKE is HIGH for all commands shown.
2. A0–A11 define the op-code written to the mode register, and A12 should be driven LOW.
3. A0–A12 provide row address, and BA0, BA1 determine which bank is made active.
4. A0–A9, A11 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

CKE Truth Table – 1/, 2/, 3/, 4/

CKE_{n-1}	CKE_n	Current State	$COMMAND_n$	$ACTION_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Clock suspend	X	Maintain clock suspend	
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Clock suspend	X	Exit clock suspend	6
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All banks idle	Auto refresh		
		Reading or writing	Valid	Clock suspend entry	
H	H		See Current State Bank n, Command to Bank n Truth Table		

1. CKEn is the logic state of CKE at clock edge n; CKEn - 1 was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge n will put the device in the all banks idle state in time for clock edge n + 1 (provided that tCKS is met).
6. After exiting clock suspend at clock edge n, the device resumes operation and recognize the next command at clock edge n + 1.

FIGURE 3. Truth tables.

Current State Bank n, Command to Bank n 1/ 2/ 3/ 4/ 5/ 6/

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row Active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

Notes:
1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH and after tXSR has been met.
2. This table is bank-specific (except where noted) the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state, this table, and the Current State Bank n, Command to Bank m table.
   Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank will be in the idle state.
   Row activating: Starts with registration of an ACTIVE command and ends when tRCD is met. After tRCD is met, the bank will be in the row active state.
   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.
   Write w/auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. After tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. After tRC is met, the SDRAM will be in the all banks idle state.
   Accessing mode register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. After tMRD is met, the SDRAM will be in the all banks idle state.
   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. After tRP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

FIGURE 3. Truth tables - continued.

Current State Bank n, Command to Bank m 1/ 2/ 3/ 4/ 5/ 6/

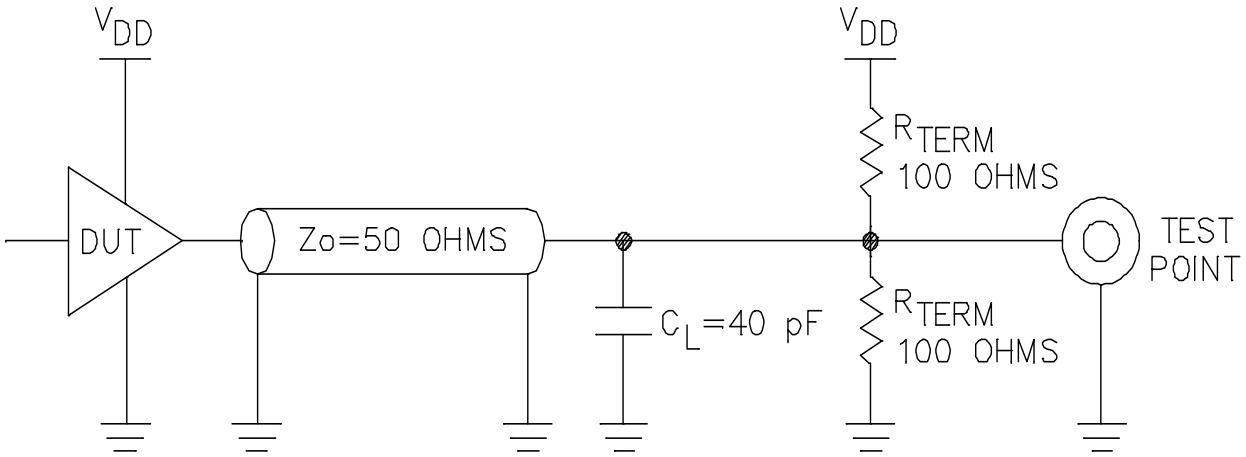
Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to Bank m	
Row activating, active, or pre-charging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7,10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7,11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7,12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7,13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7,8,14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7,8,15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7,8,16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7,8,17
	L	L	H	L	PRECHARGE	9

Notes:
1. This table applies when CKEn - 1 was HIGH and CKEn is HIGH (see CKE truth table) and after tXSR has been met.
2. This table describes alternate bank operation except where noted; the current state is for bank n and the commands shown are those allowed to be issued to bank m (assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled, and ends when tRP has been met. After tRP is met, the enabled: bank will be in the idle state.
   Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when tRP has been met. After tRP is met, the bank will be in the idle state.
4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank m listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank n initiates the auto precharge command when its burst has been interrupted by bank m's burst.
9. Burst in bank n continues as initiated.

FIGURE 3. Truth tables - continued.

10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m interrupts the READ on bank n, CL later (Figure 5, Timing waveforms, Consecutive READ Bursts).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m interrupts the READ on bank n when registered (Figure 5, Timing waveforms, READ-to-WRITE and READ-to-WRITE with Extra Clock Cycle). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m interrupts the WRITE on bank n when registered (Figure 5, Timing waveforms, WRITE-to-READ), with the data-out appearing CL later. The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m interrupts the WRITE on bank n when registered (Figure 5, Timing waveforms, WRITE-to-WRITE). The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m interrupts the READ on bank n, CL later. The PRECHARGE to bank n will begin when the READ to bank m is registered (Figure 5, Timing waveforms, READ with Auto Precharge Interrupted by a READ).
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m interrupts the READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank n will begin when the WRITE to bank m is registered (Figure 5, Timing waveforms, READ with Auto Precharge Interrupted by a WRITE).
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m interrupts the WRITE on bank n when registered, with the data-out appearing CL later. The PRECHARGE to bank n will begin after tWR is met, where tWR begins when the READ to bank m is
registered. The last valid WRITE to bank n will be data in registered one clock prior to the READ to bank m (Figure 5, Timing waveforms, WRITE with Auto Precharge Interrupted by a READ).
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m interrups the WRITE on bank n when registered. The PRECHARGE to bank n begins after tWR is met, where tWR begins when the WRITE to bank m is registered. The last valid WRITE to bank n will be data registered one clock prior to the WRITE to bank m (Figure 5, Timing waveforms, WRITE with Auto Precharge Interrupted by a WRITE).

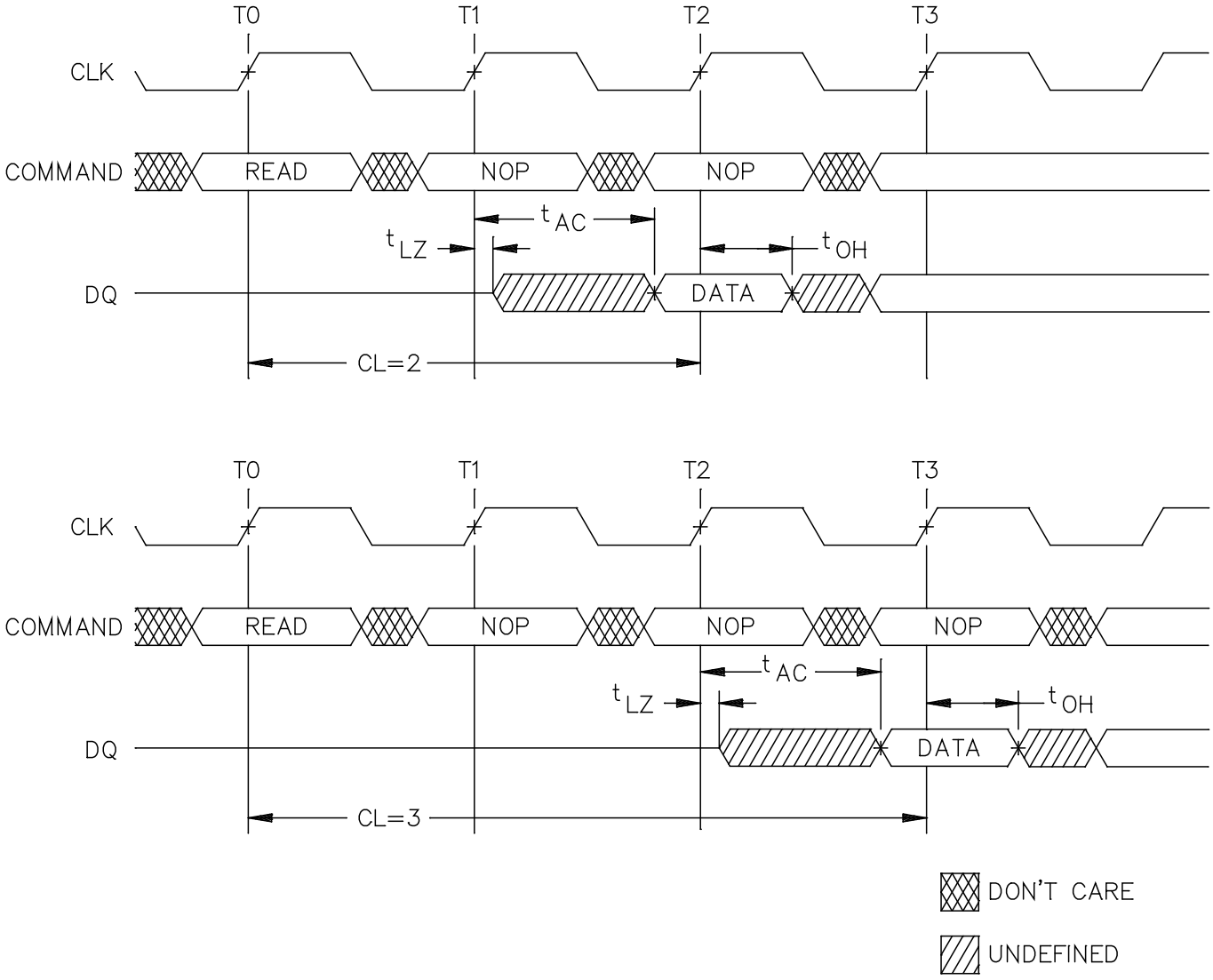
FIGURE 3. Truth tables - continued.



Note: C_L = 40 pF including scope probe and test socket.

FIGURE 4. Output load circuit

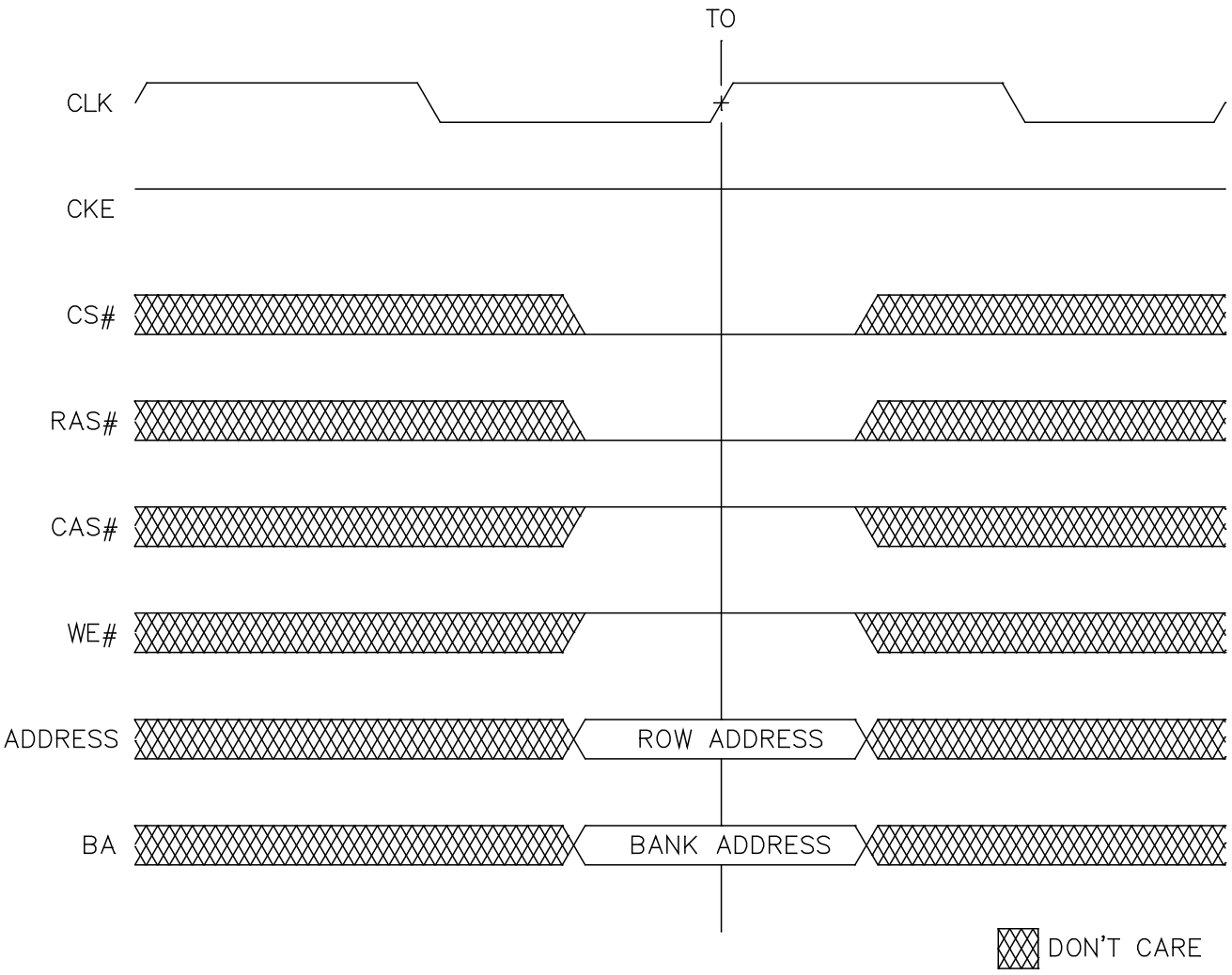
CAS latency



Allowable operating frequency (MHz)	
Frequency	Latency
≤ 100	CL = 2

FIGURE 5. Timing waveforms.

Activating a specific row in a specific bank



Example meeting t_{RCD}(Min) when $2 < t_{RCD}(Min)/t_{CK} \leq 3$.

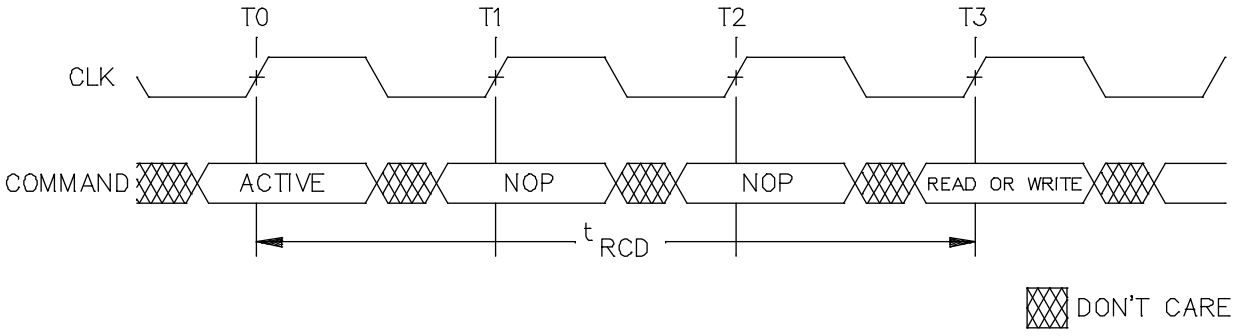


FIGURE 5. Timing waveforms - continued.

READ command

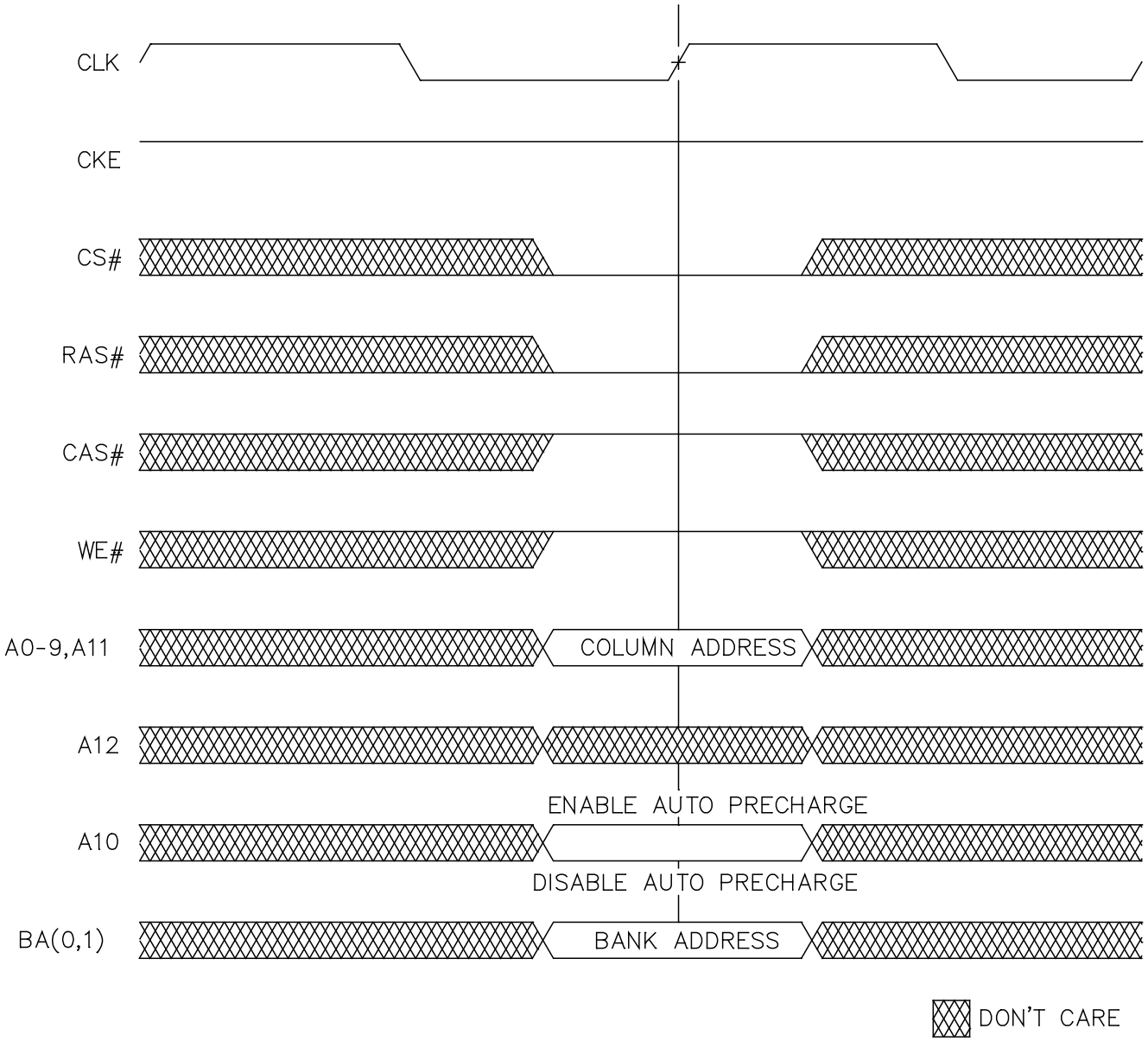
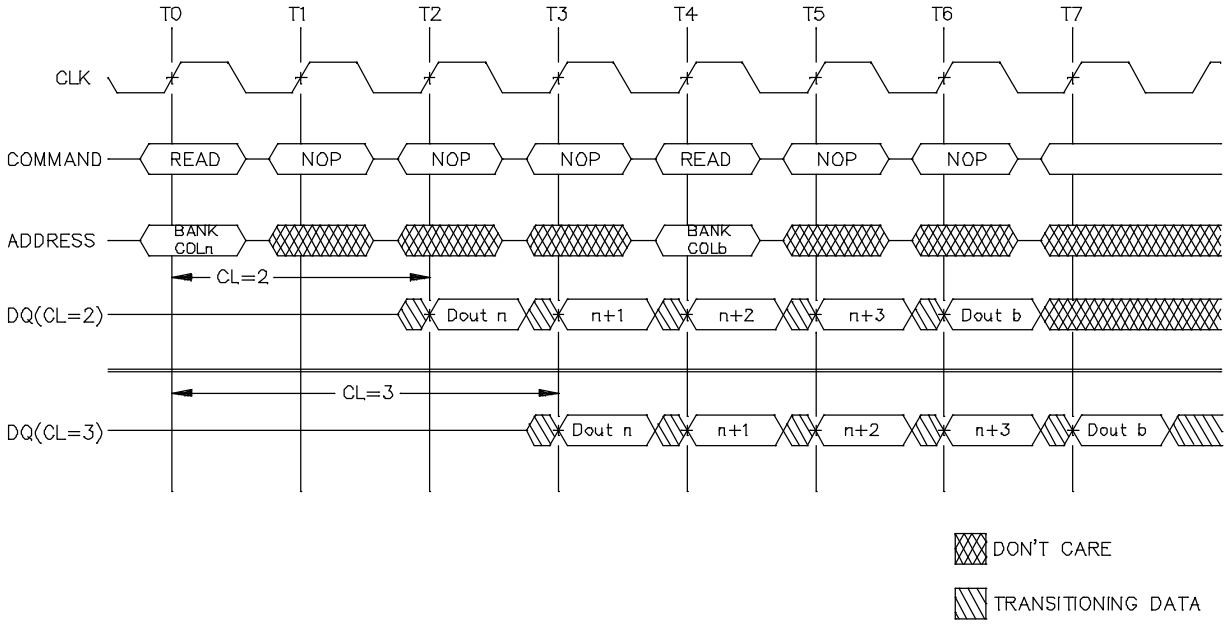


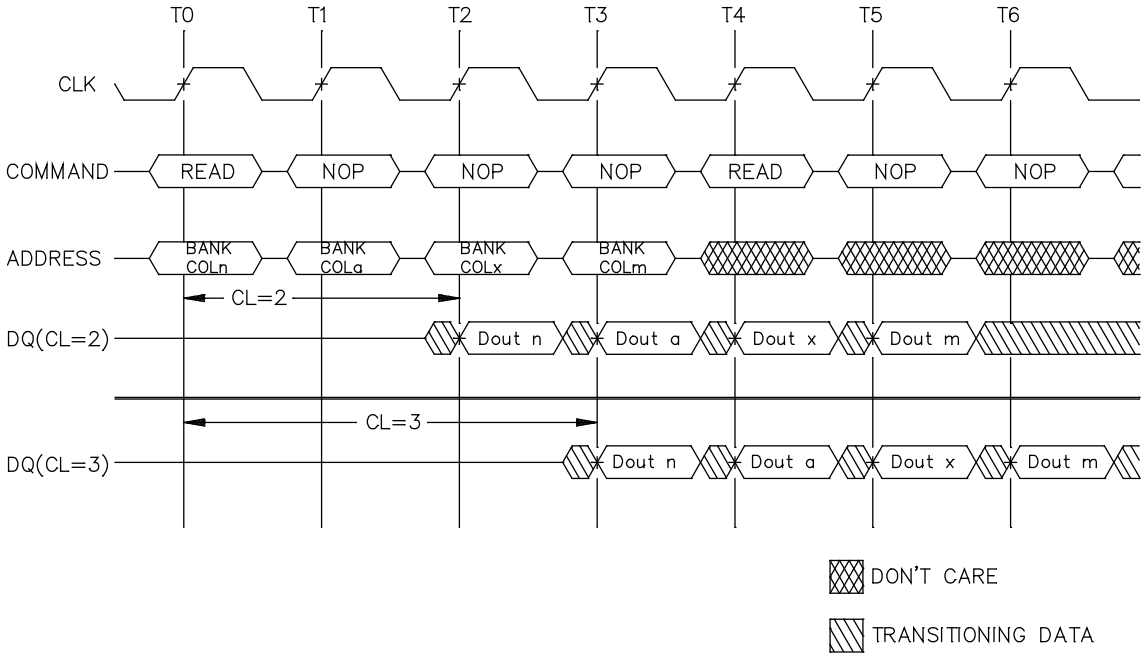
FIGURE 5. Timing waveforms - continued.

Consecutive READ bursts



Note: 1. Each READ command may be to any bank. DQM is Low.

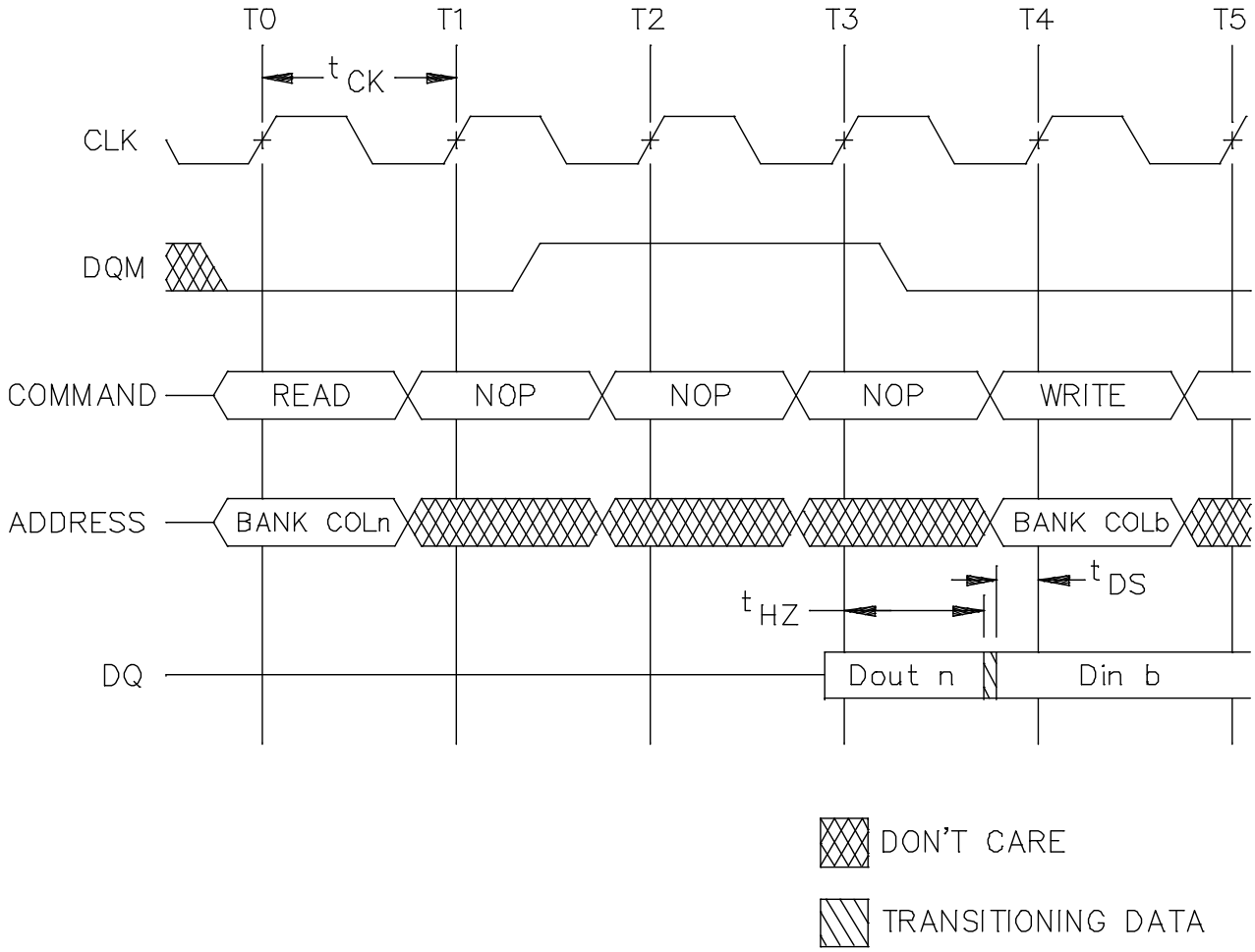
Random READ accesses



Note: 1. Each READ command may be to any bank. DQM is Low.

FIGURE 5. Timing waveforms - continued.

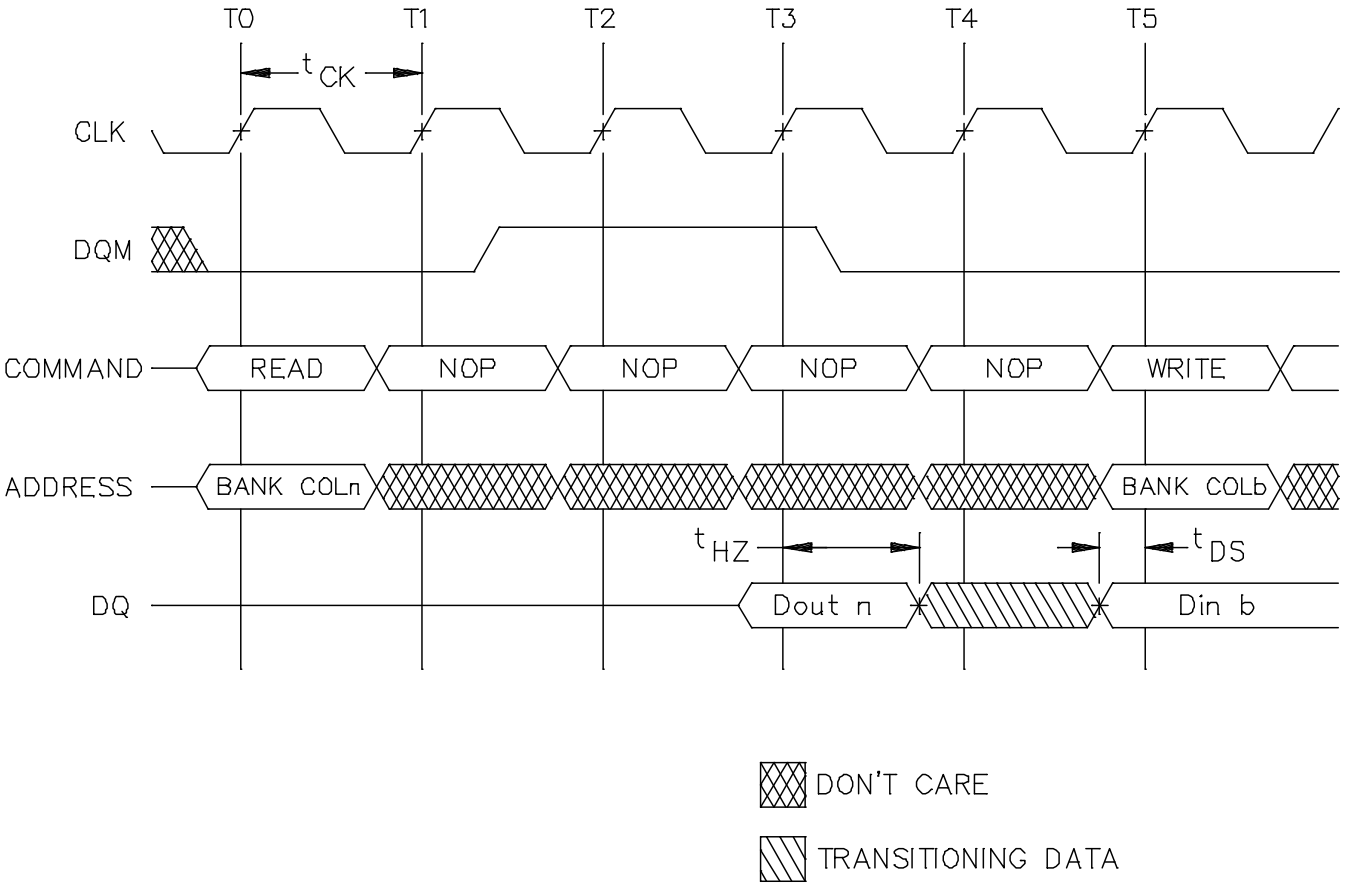
READ to WRITE



Note: CL = 3 is used for illustration. The READ and WRITE command may be to any bank. If a burst of one is used, DQM is not required.

FIGURE 5. Timing waveforms - continued.

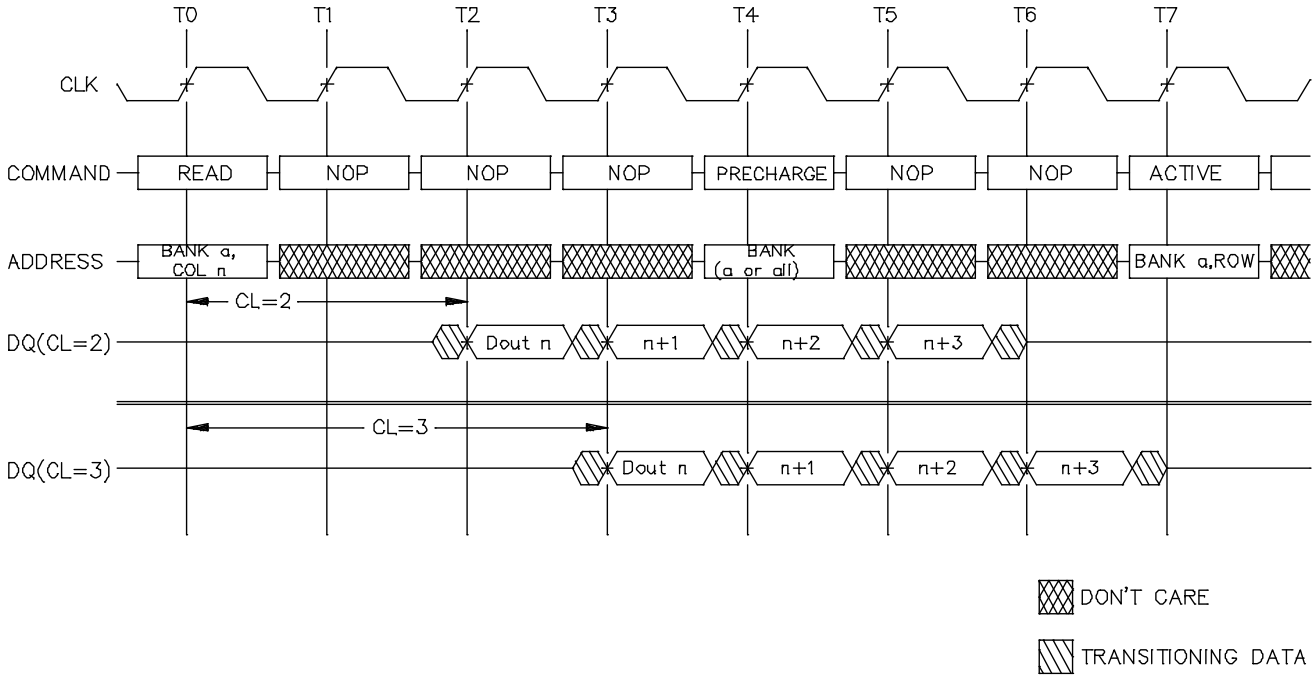
READ to WRITE with extra clock cycle



Note: CL = 3 is used for illustration. The READ and WRITE command may be to any bank. If a burst of one is used, DQM is not required.

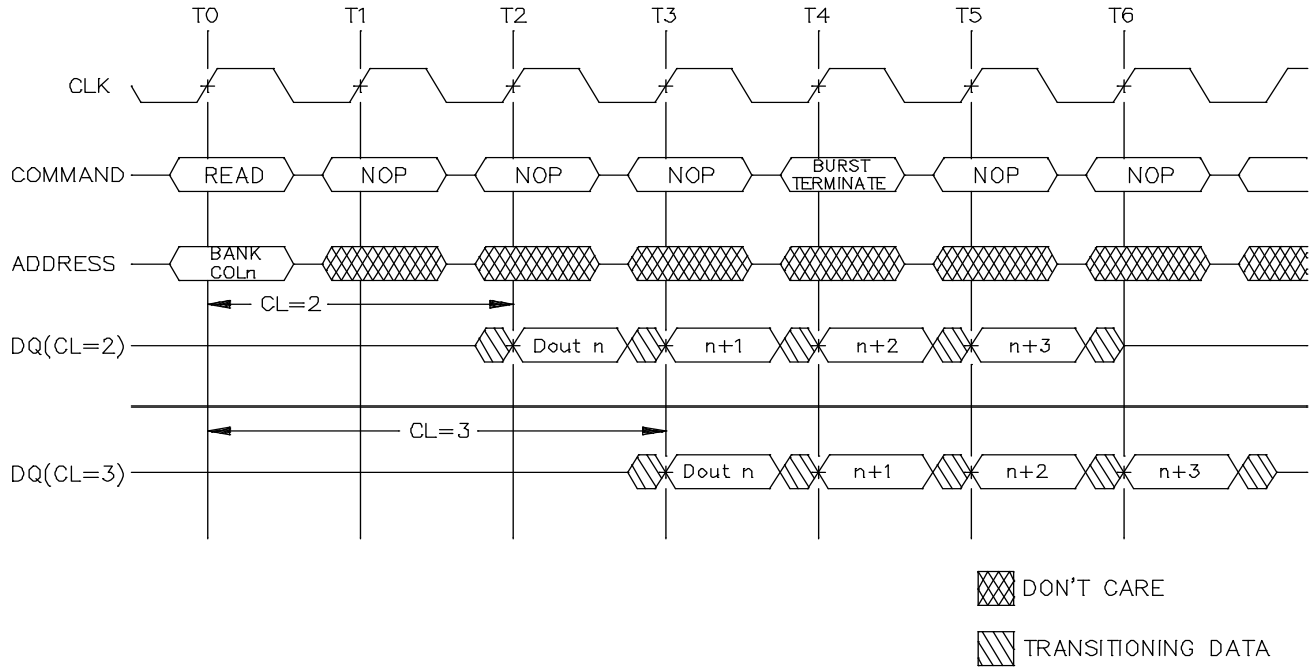
FIGURE 5. Timing waveforms - Continued.

READ to PRECHARGE



Note: DQM is Low.

Terminating a READ burst



Note: DQM is Low.

FIGURE 5. Timing waveforms - continued.

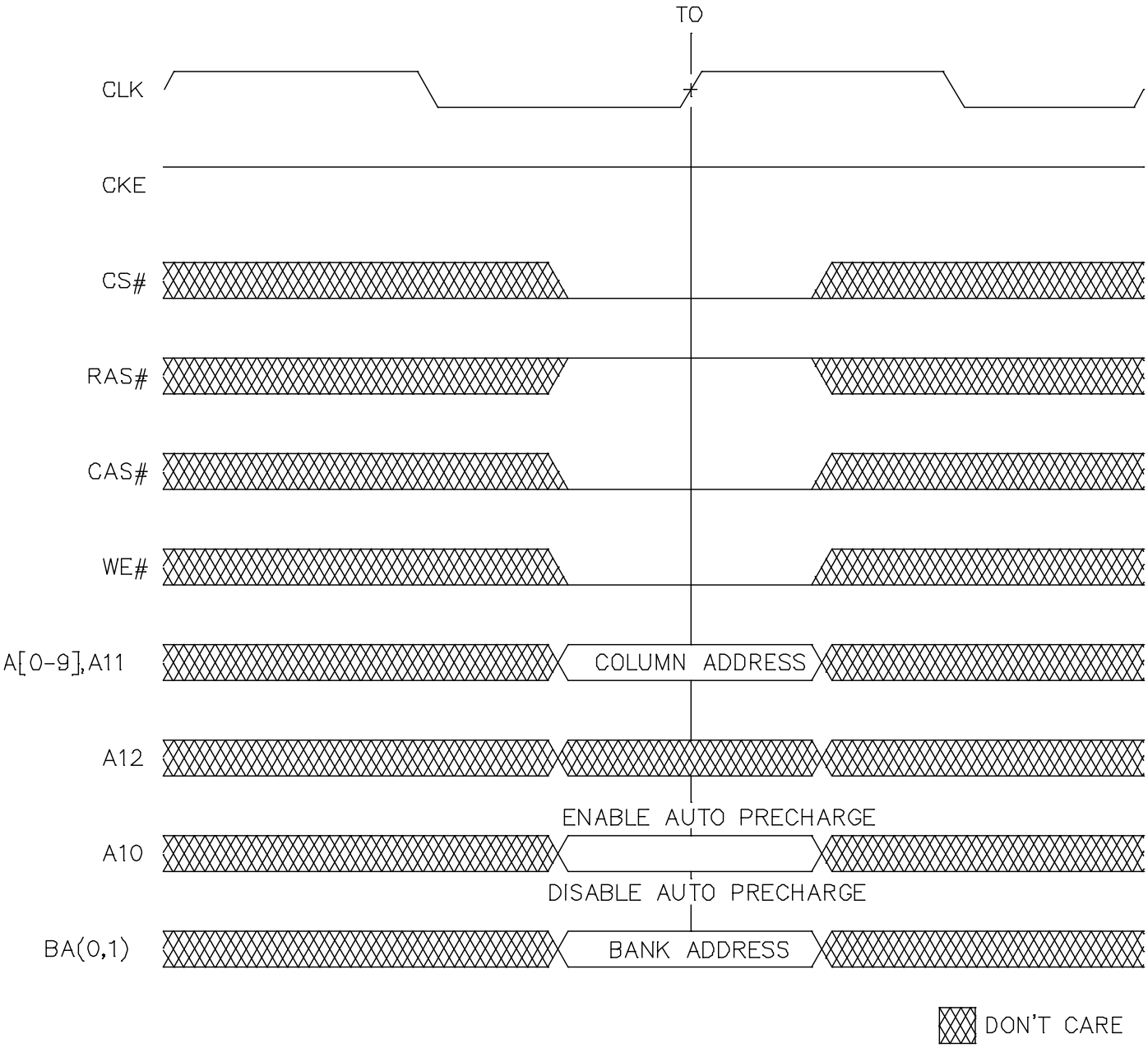
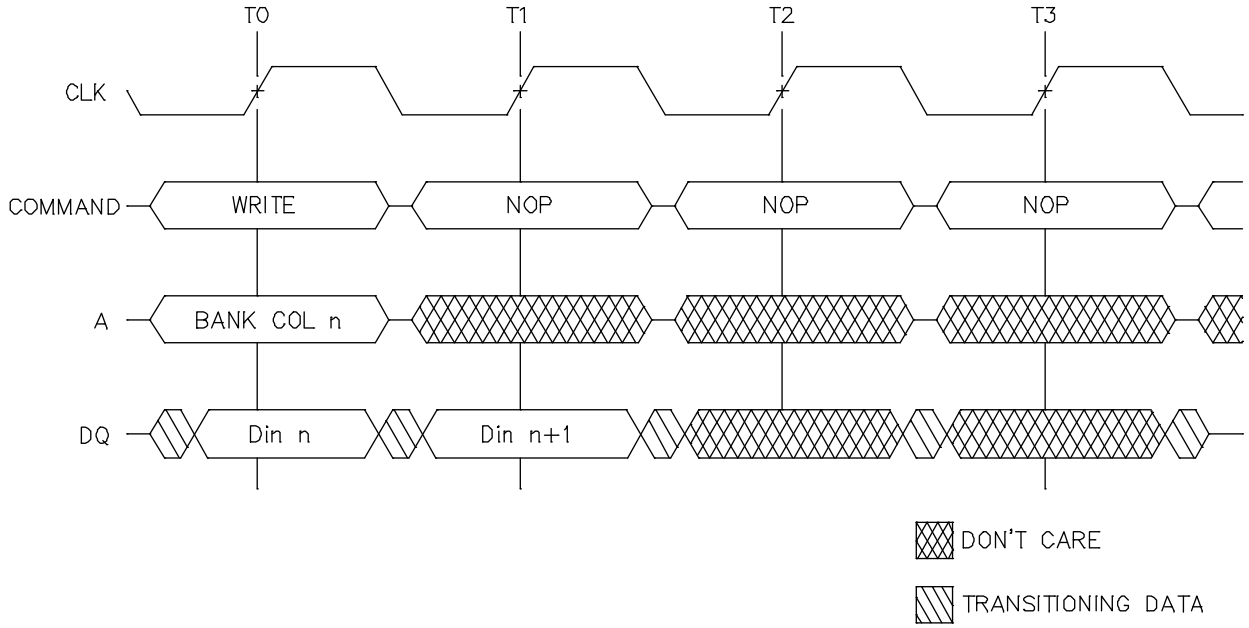


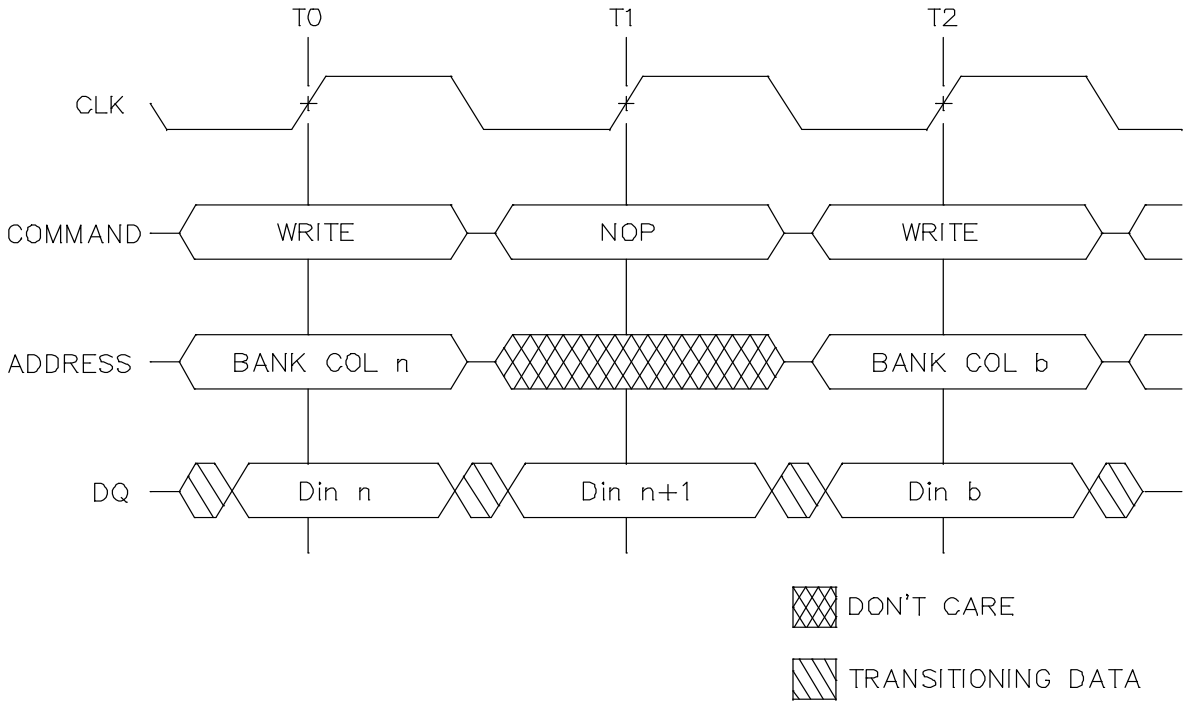
FIGURE 5. Timing waveforms - continued.

Write burst



Note: BL = 2, DQM is Low.

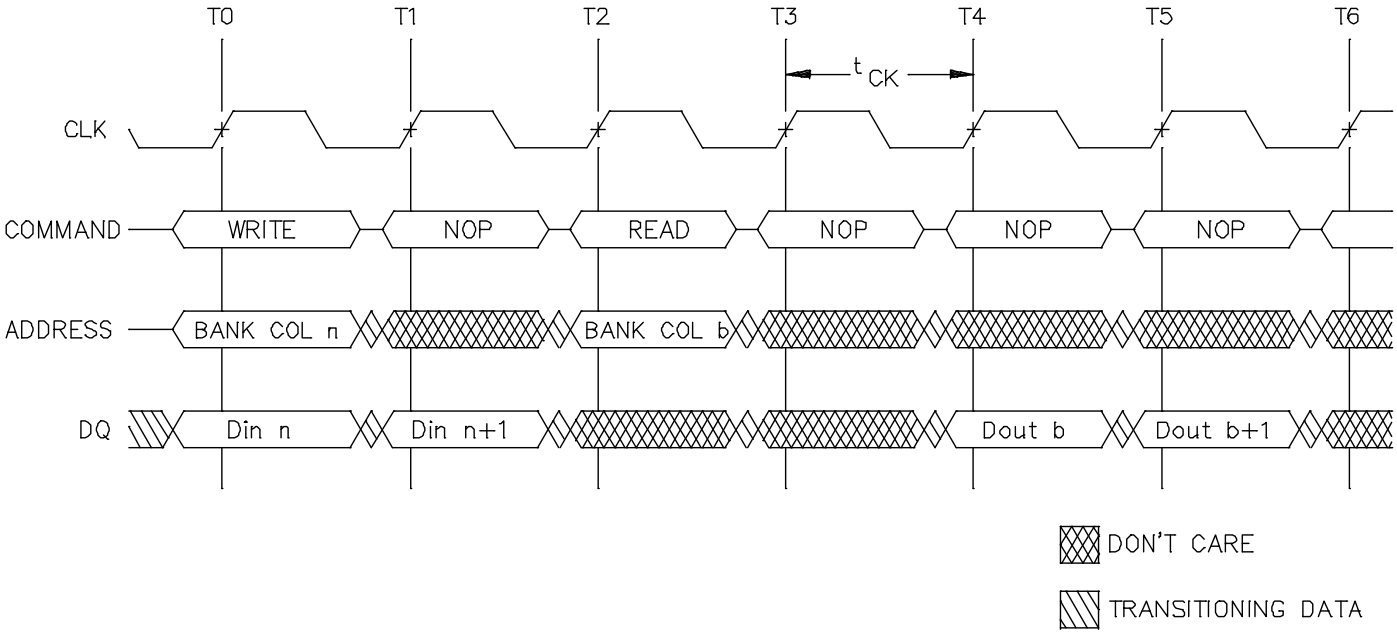
WRITE to WRITE



Note: DQM is Low. Each WRITE command may be to any bank.

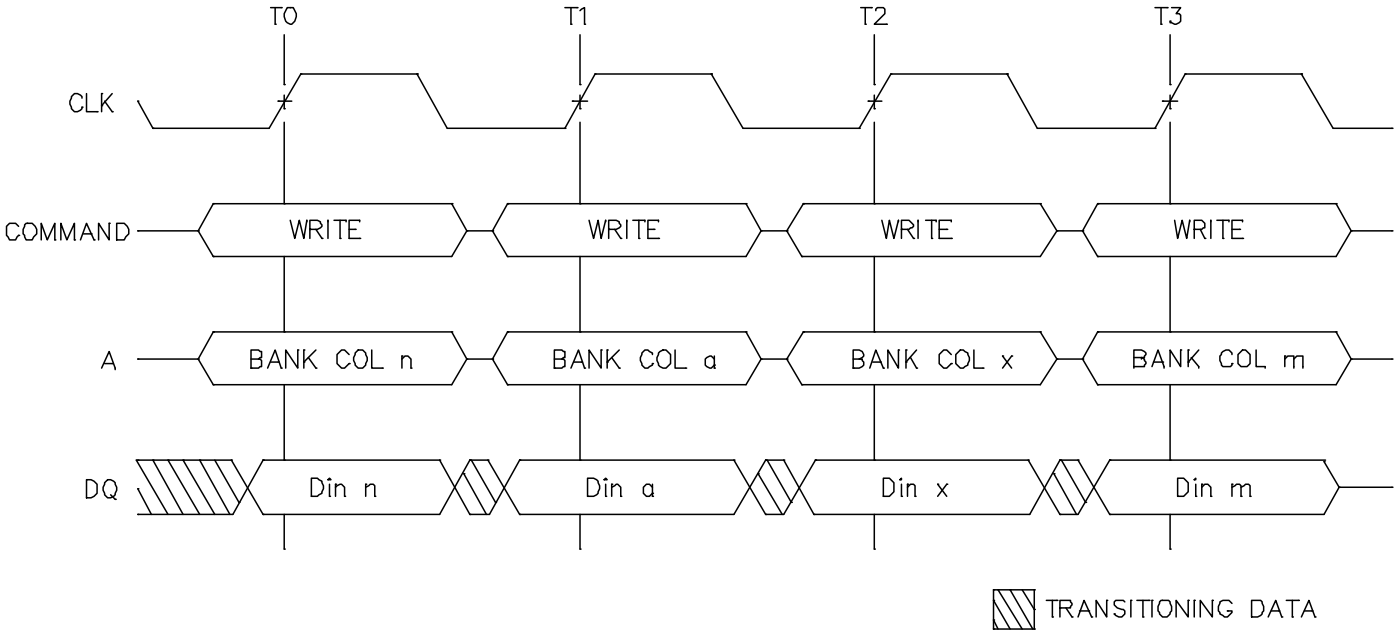
FIGURE 5. Timing waveforms - continued.

WRITE to READ



Note: DQM is Low. Each WRITE command may be to any bank.

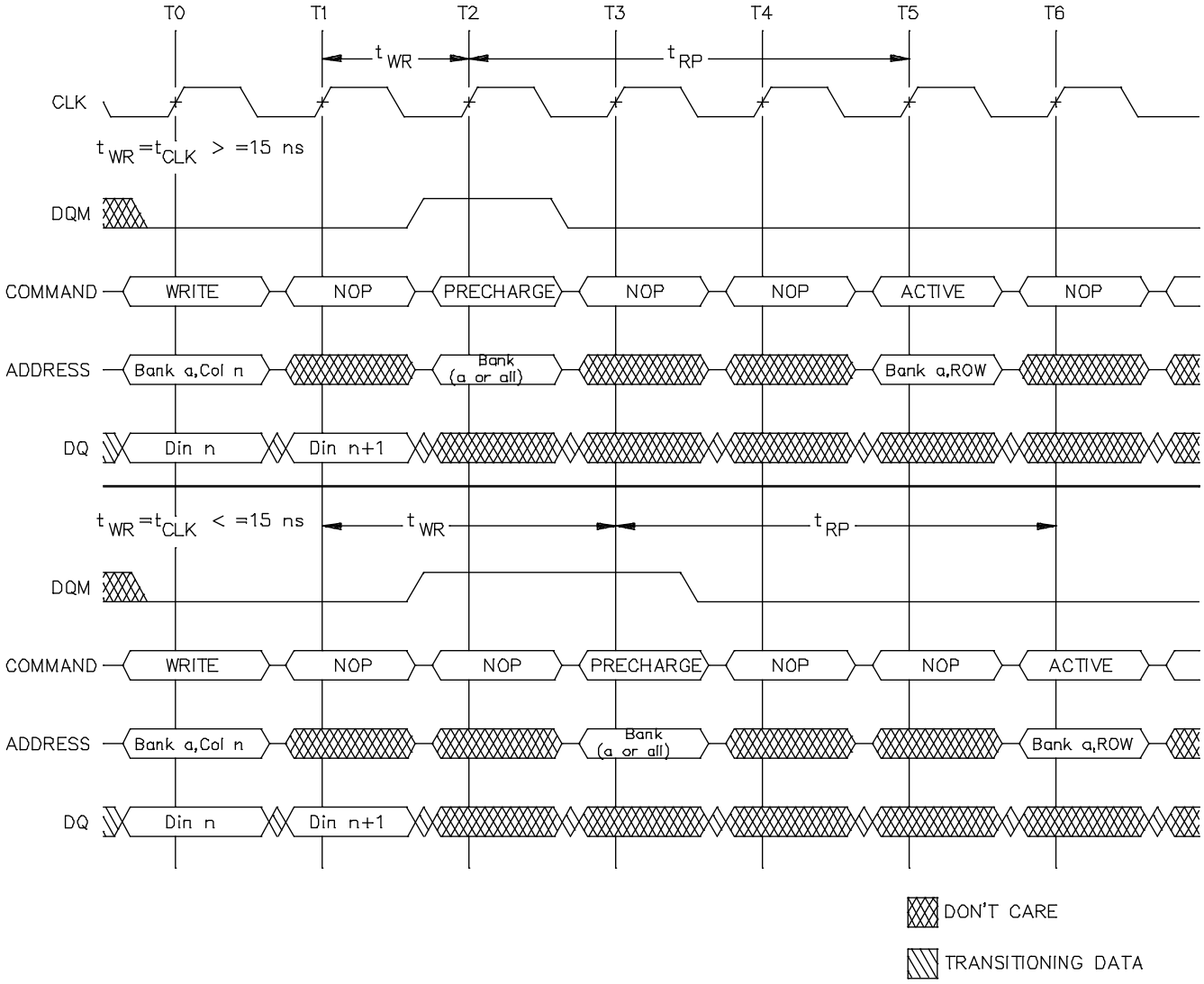
Random WRITE cycles



Notes: The WRITE or READ command any be to any bank. DQM is Low.

FIGURE 5. Timing waveforms - continued.

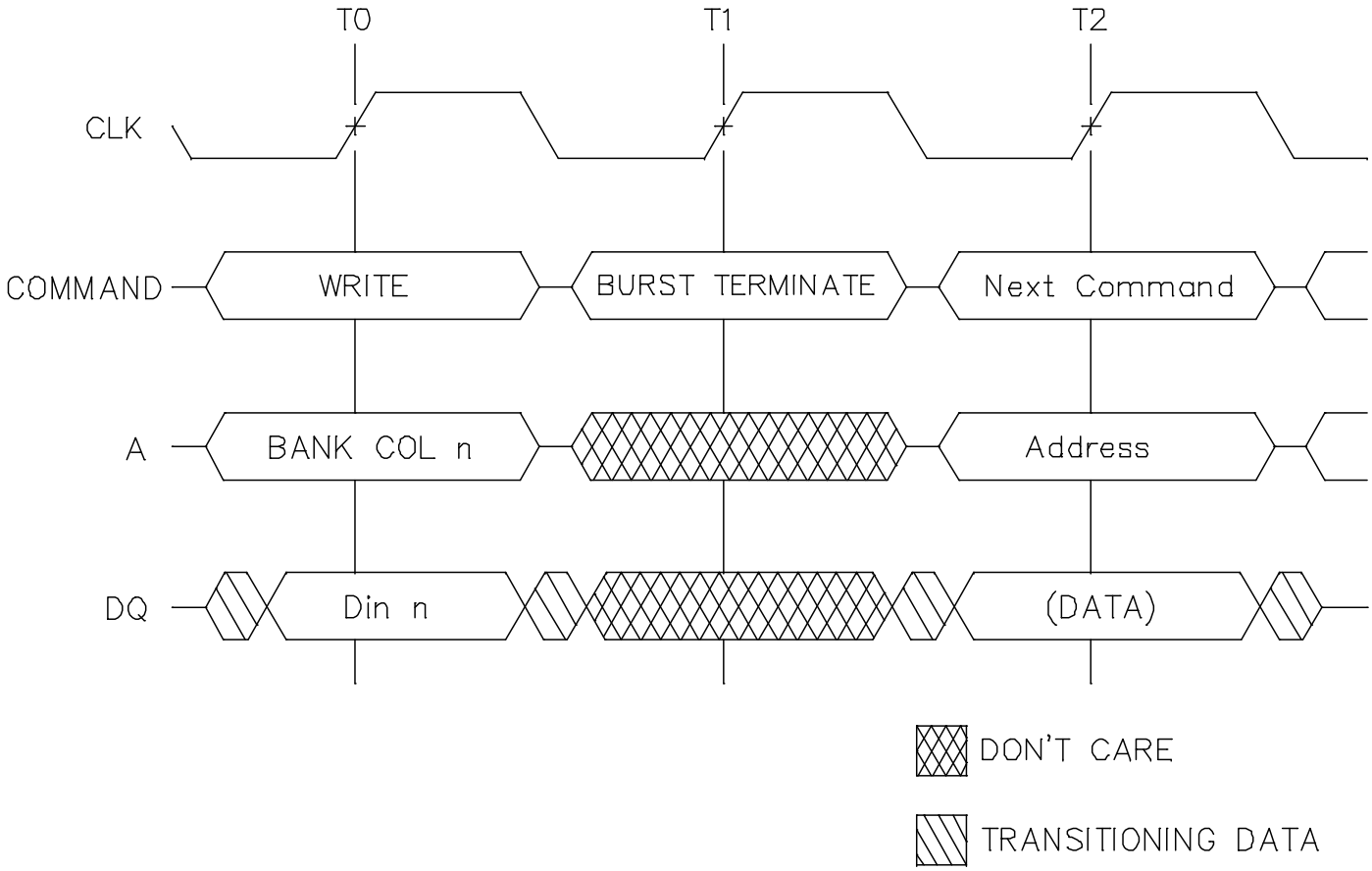
WRITE to PRECHARGE



Note: DQM could remain low in this example if the write burst is a fixed length of two.

FIGURE 5. Timing waveforms - Continued.

Terminating a Write burst



Note: DQMs are Low.

FIGURE 5. Timing waveforms – Continued.

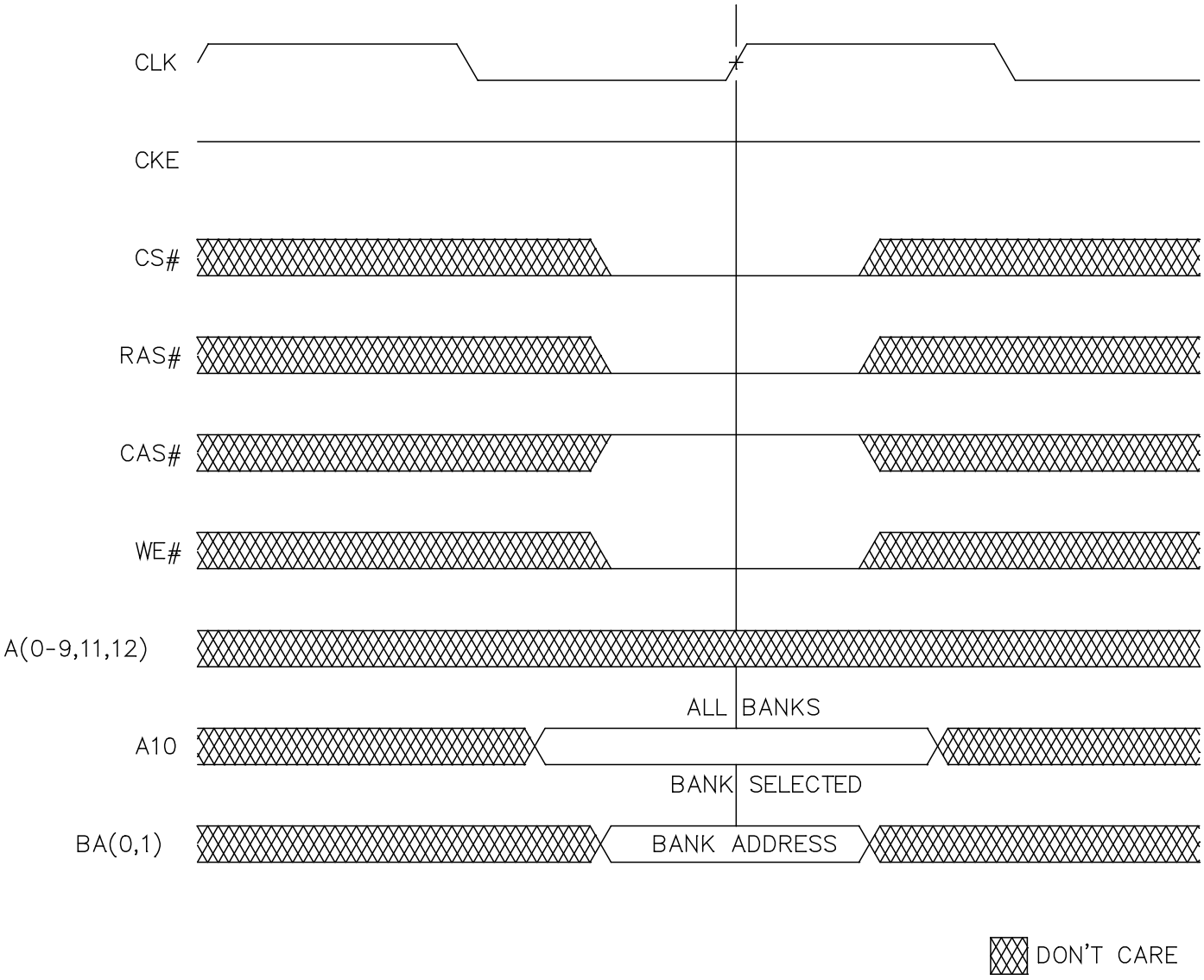


FIGURE 5. Timing waveforms – continued.

Power Down

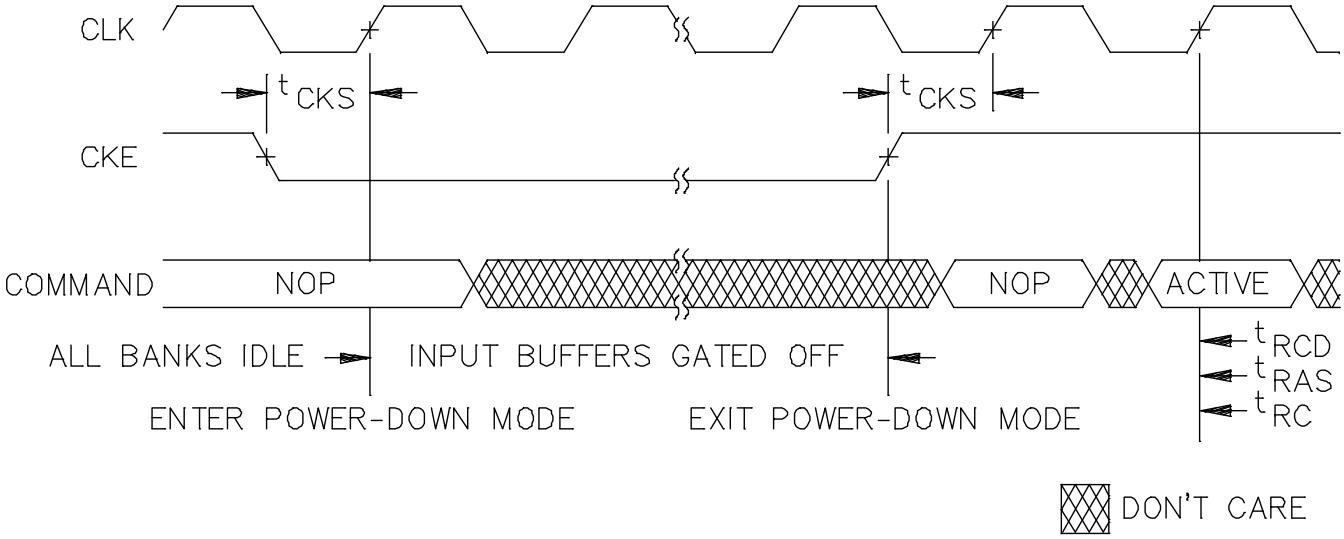
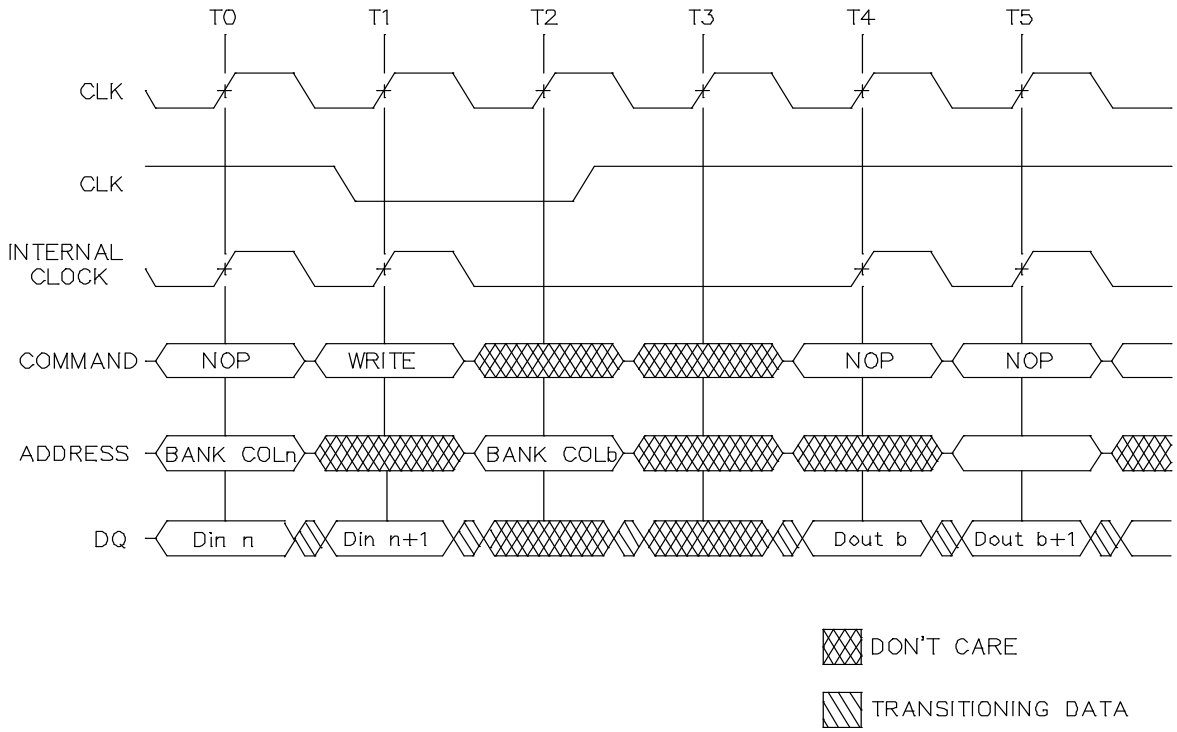


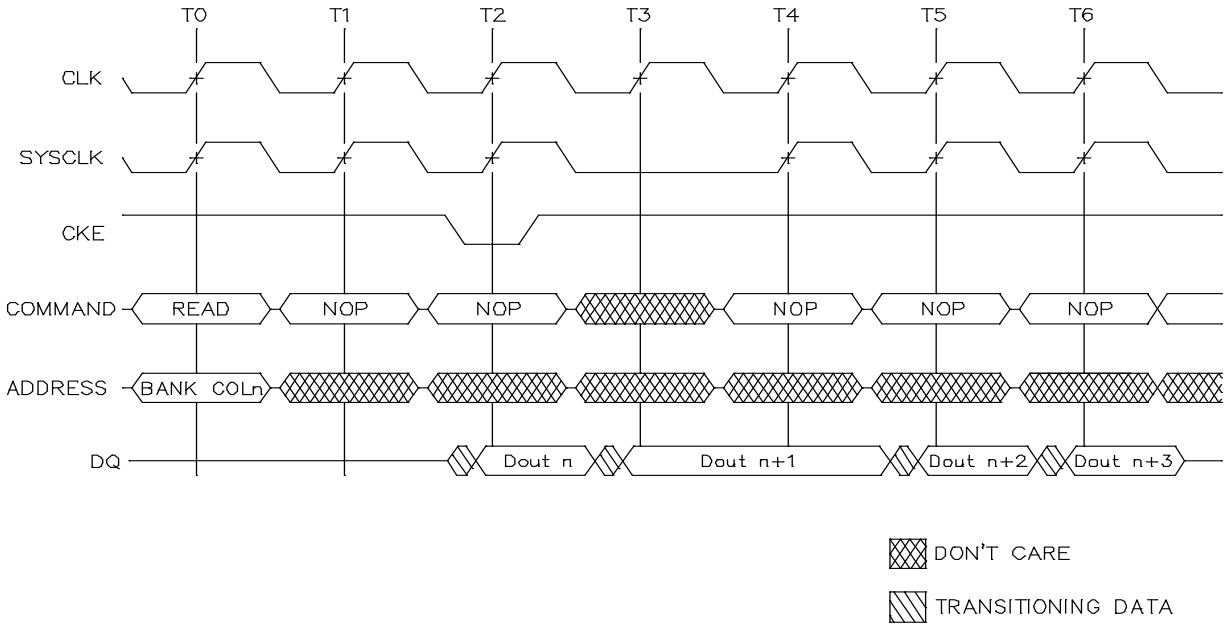
FIGURE 5. Timing waveforms – Continued.

Clock suspend during WRITE burst



Note: BL = 4 or greater, DQM is Low.

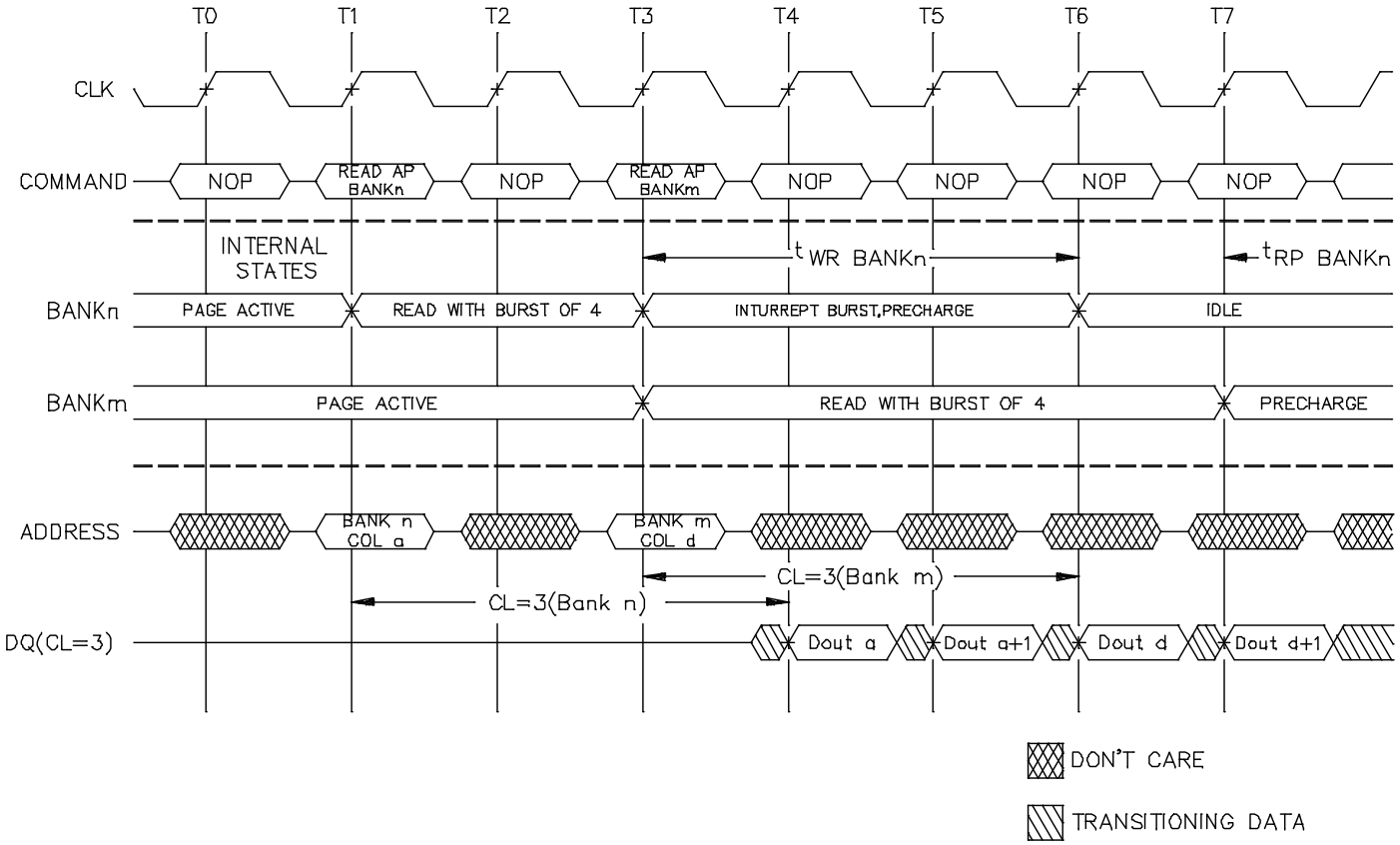
Clock suspend during READ burst



Note: For this example, CL = 2, BL = 4 or greater, DQM is Low.

FIGURE 5. Timing waveforms - Continued.

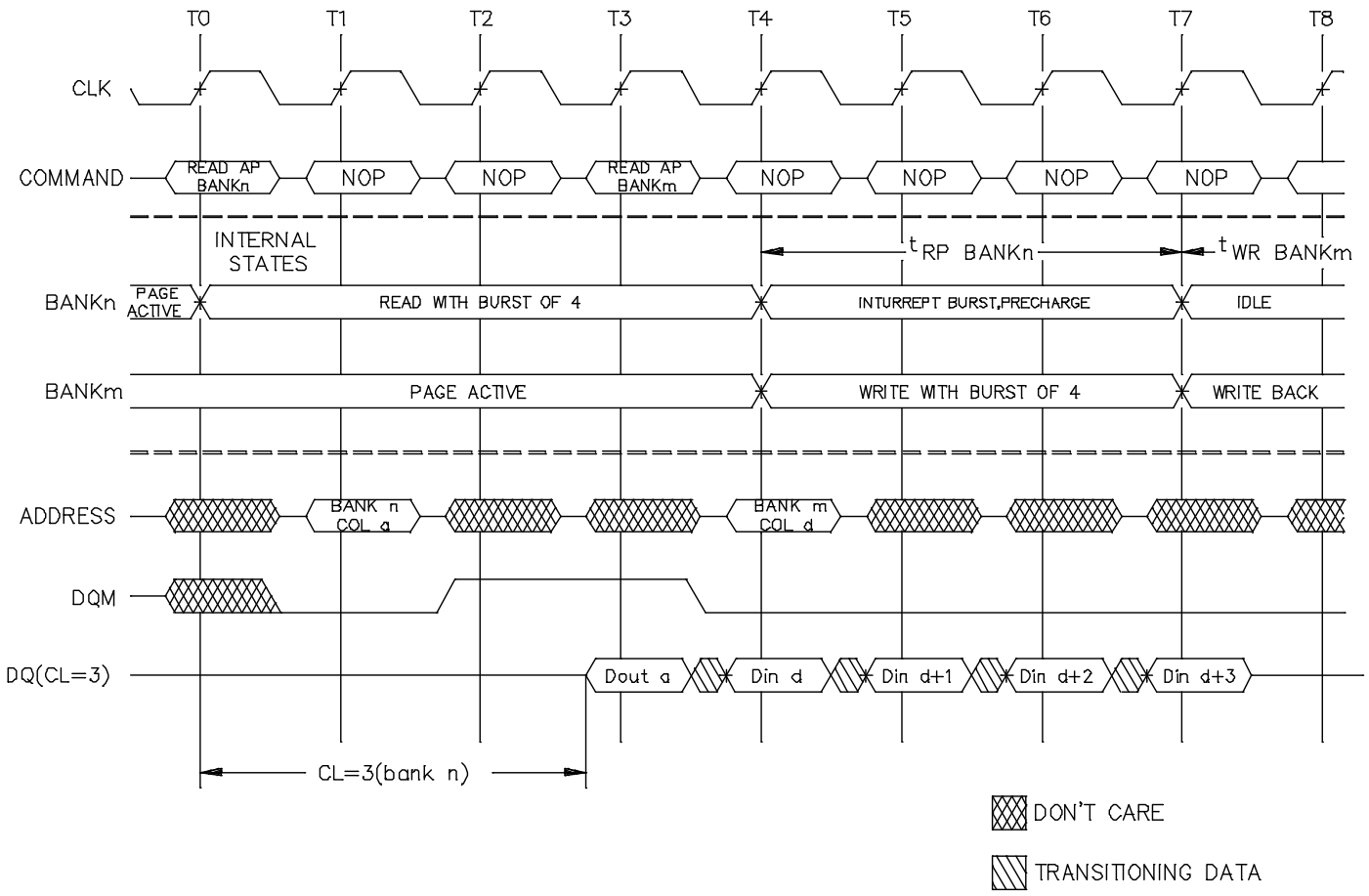
READ with auto precharge interrupted by a READ



Note: DQM is low.

FIGURE 5. Timing waveforms - Continued.

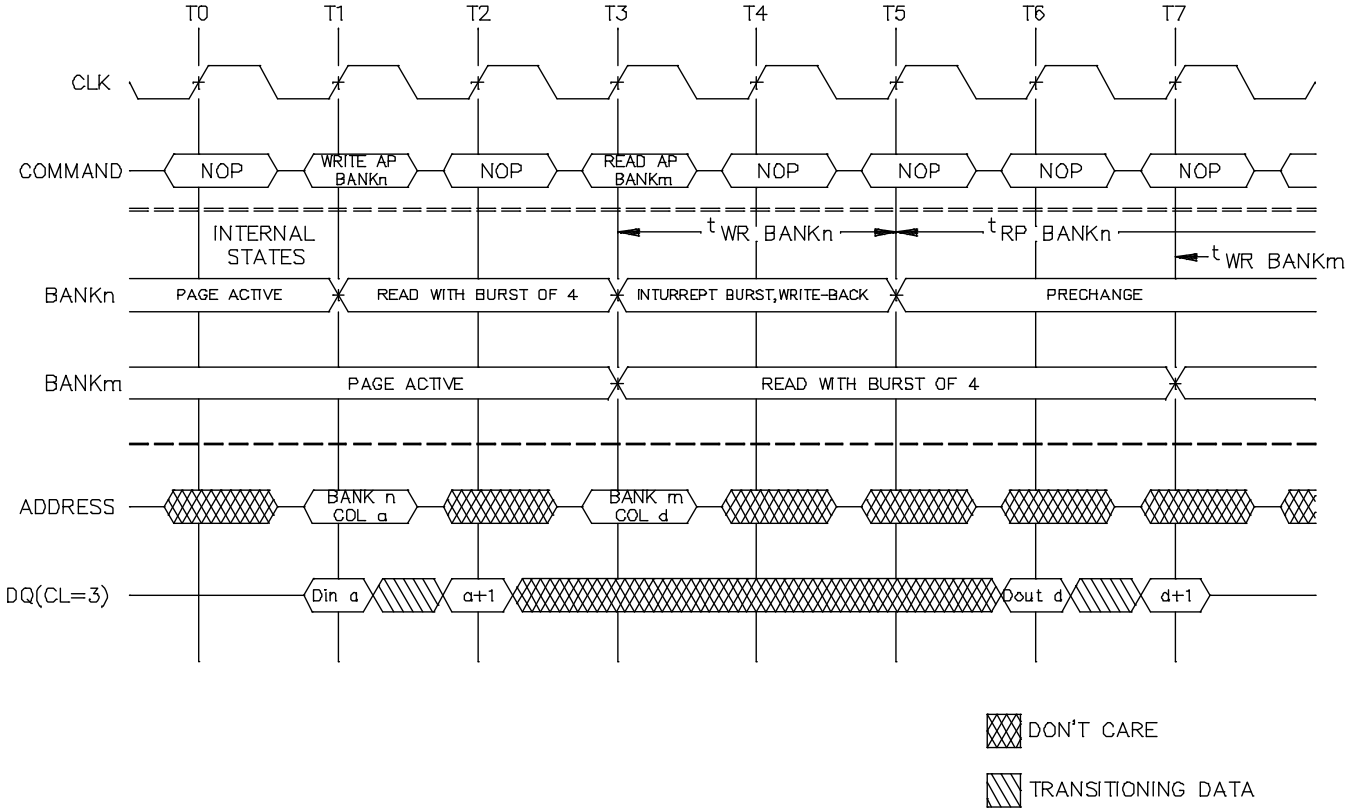
READ with auto precharge interrupted by a WRITE



Note: DQM is high at T2 to prevent D_{out} a+1 from contending with D_{in} d at T4.

FIGURE 5. Timing waveforms - Continued.

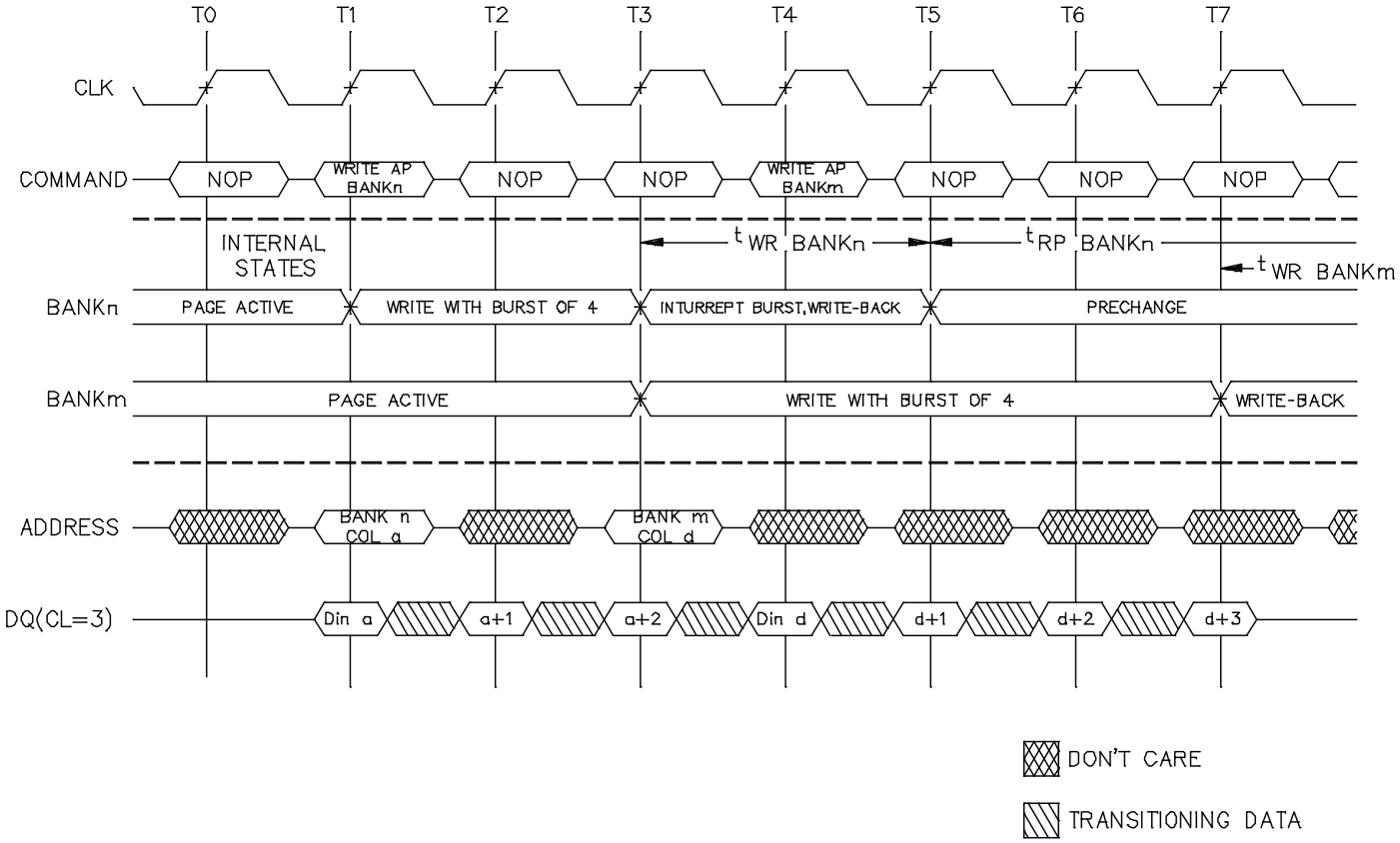
WRITE with auto precharge interrupted by a READ



Note: DQM is low.

FIGURE 5. Timing waveforms - Continued.

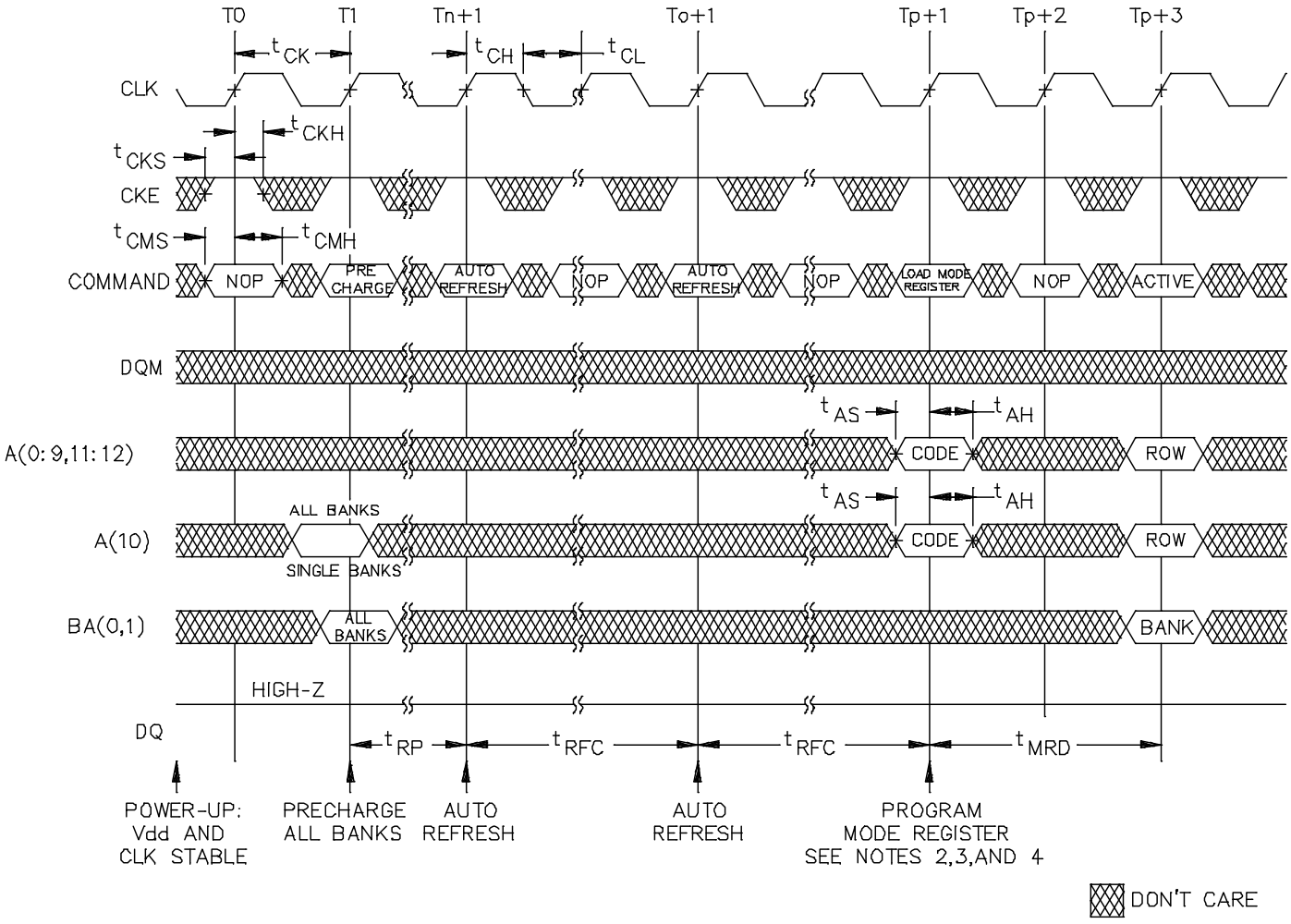
WRITE with auto precharge interrupted by a WRITE



Note: DQM is low.

FIGURE 5. Timing waveforms - Continued.

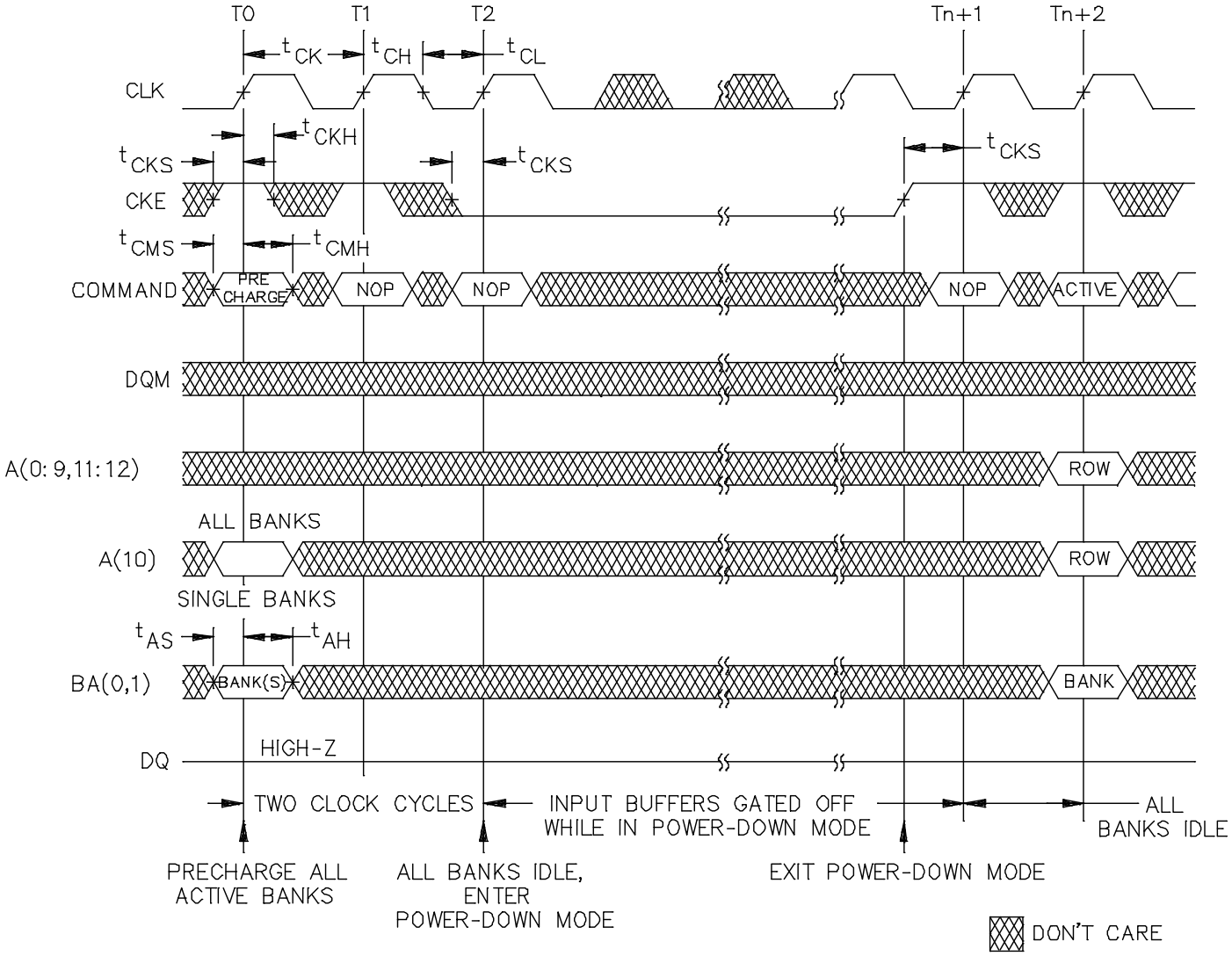
Initialize and load mode register



Notes: 1. If CS is high at clock high time, all commands applied are NOP.
2. The load register may be loaded prior to the AUTO REFRESH cycles if desired.
3. JEDEC and PC100 specify three clocks.
4. Outputs are guaranteed high-Z after command is issued.
5. A12 should be low at Tp+1.

FIGURE 5. Timing waveforms - Continued.

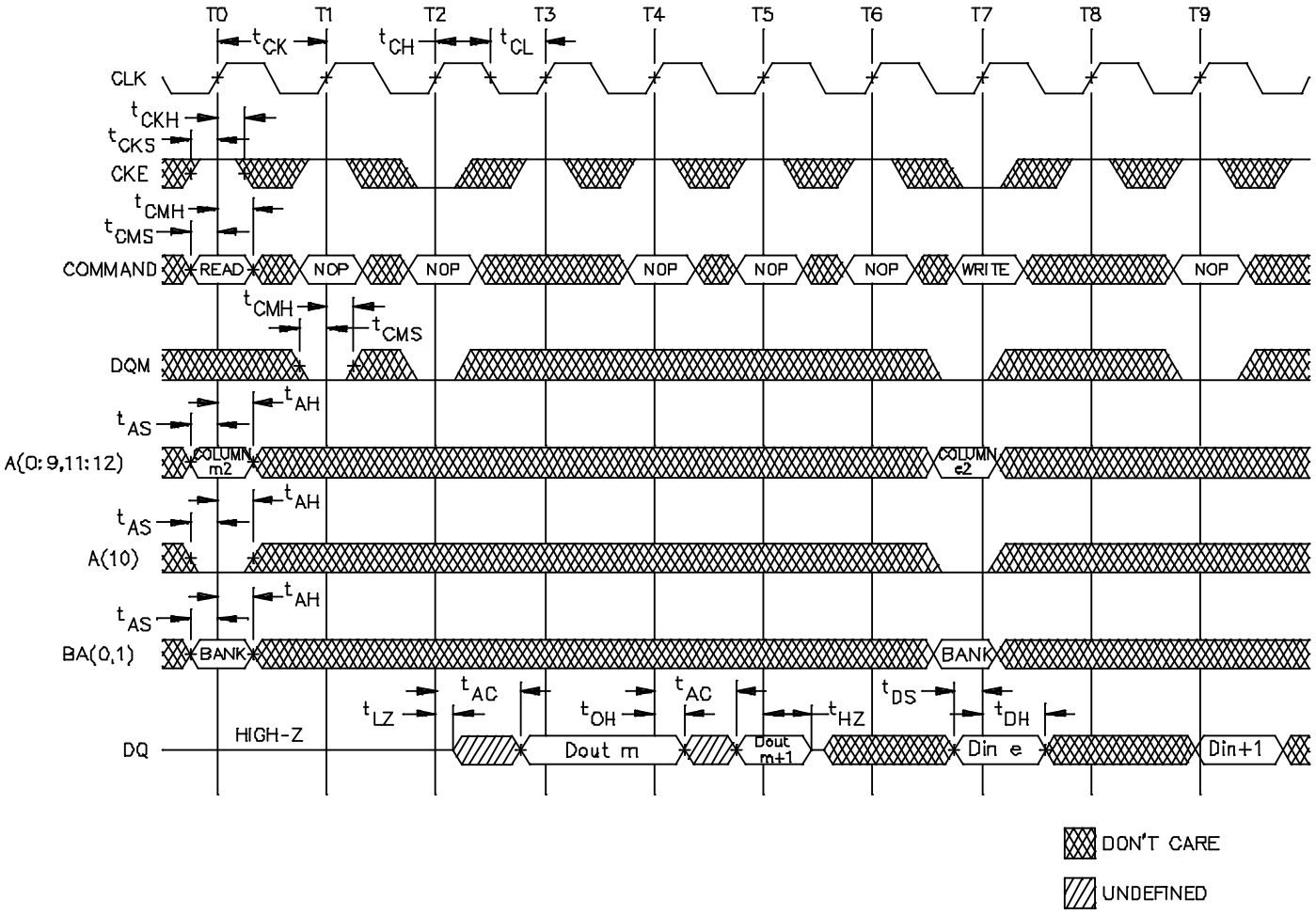
Power-down mode



Note: Violating refresh requirements during power-down may result in loss of data.

FIGURE 5. Timing waveforms - Continued.

Clock suspend mode



Notes: 1. For this example, BL = 2, CL = 3 and auto precharge is disabled.
2. A12 = “Don’t’ care”.

FIGURE 5. Timing waveforms - Continued.

Auto-refresh mode

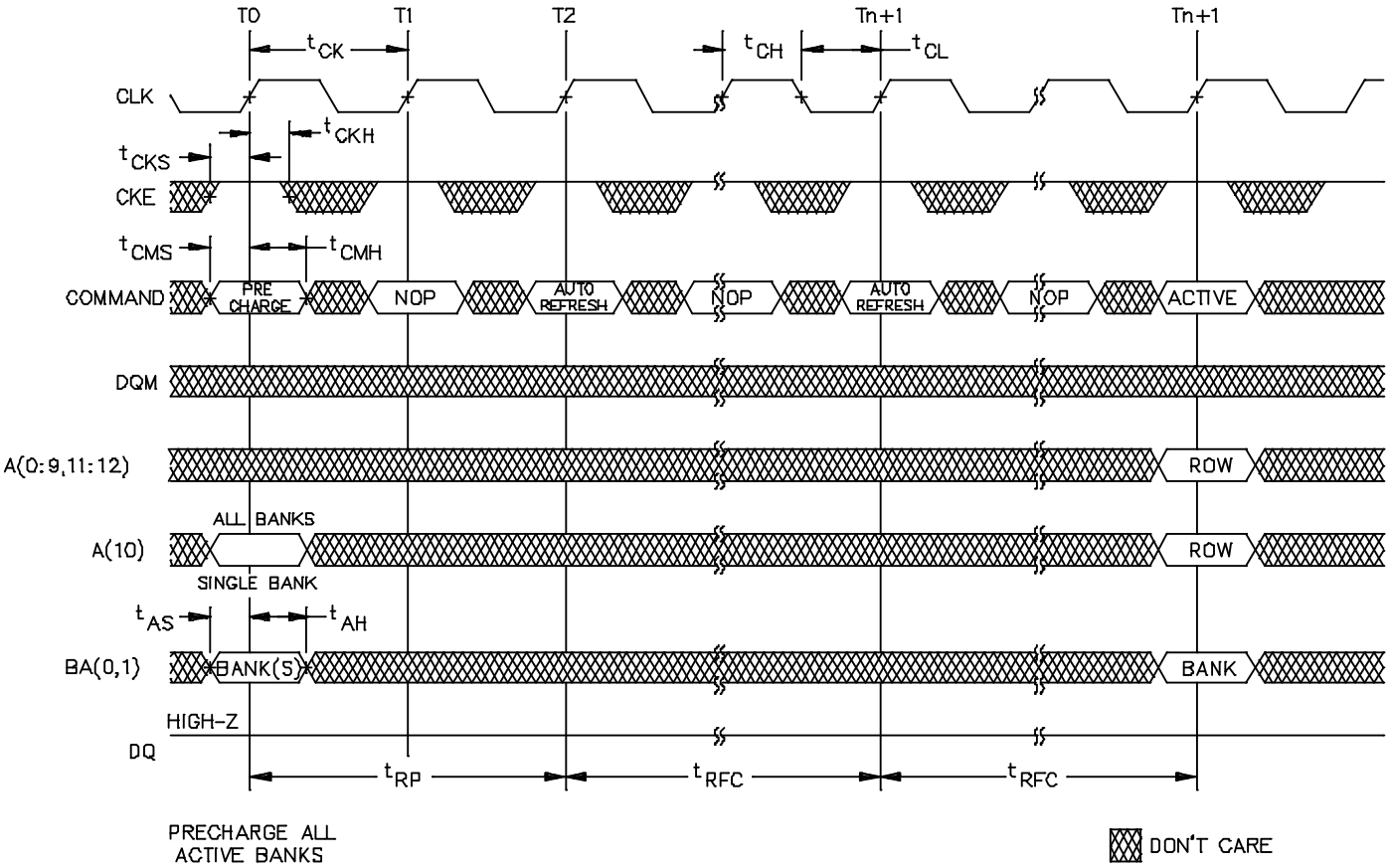
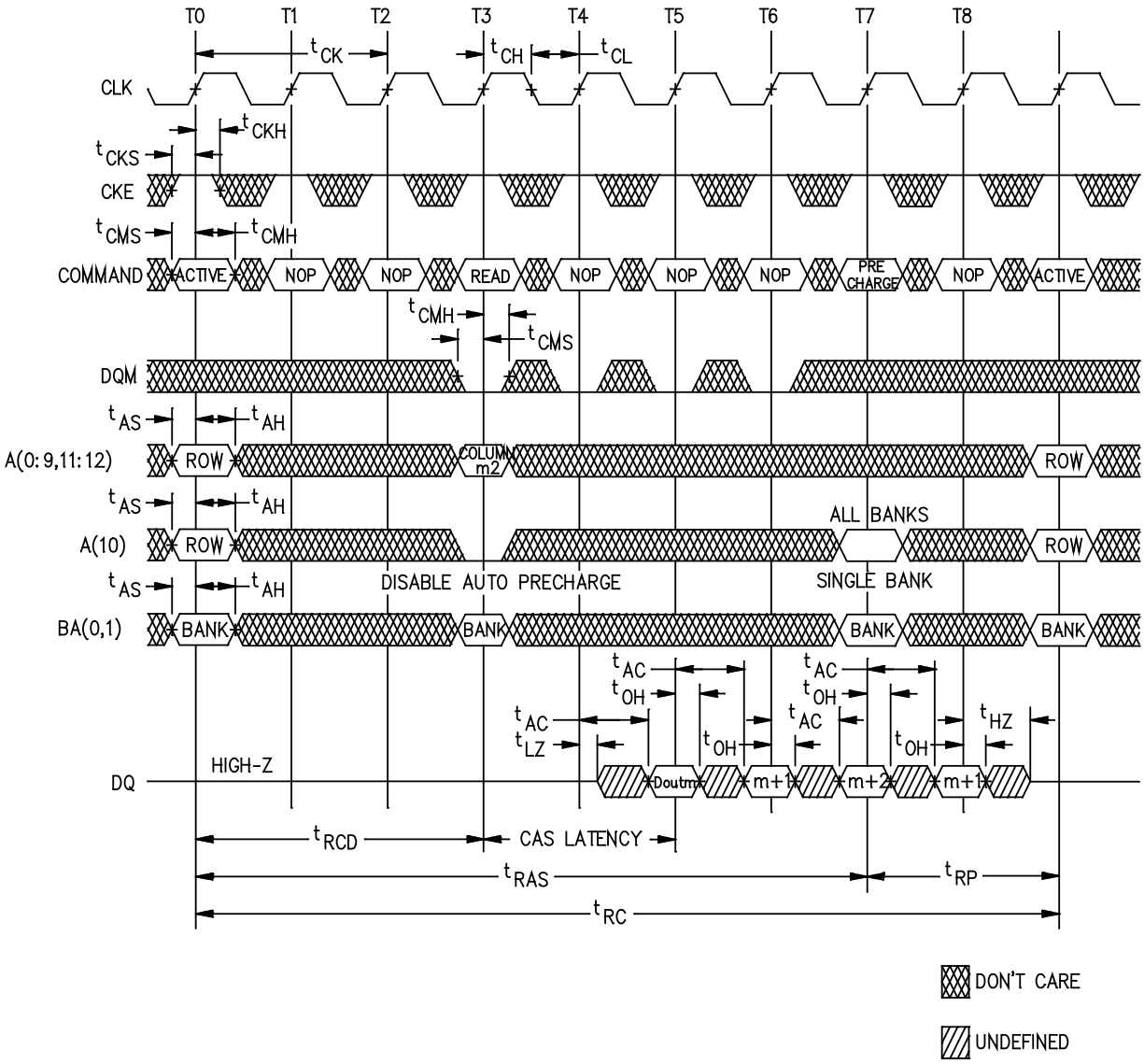


FIGURE 5. Timing waveforms - Continued.

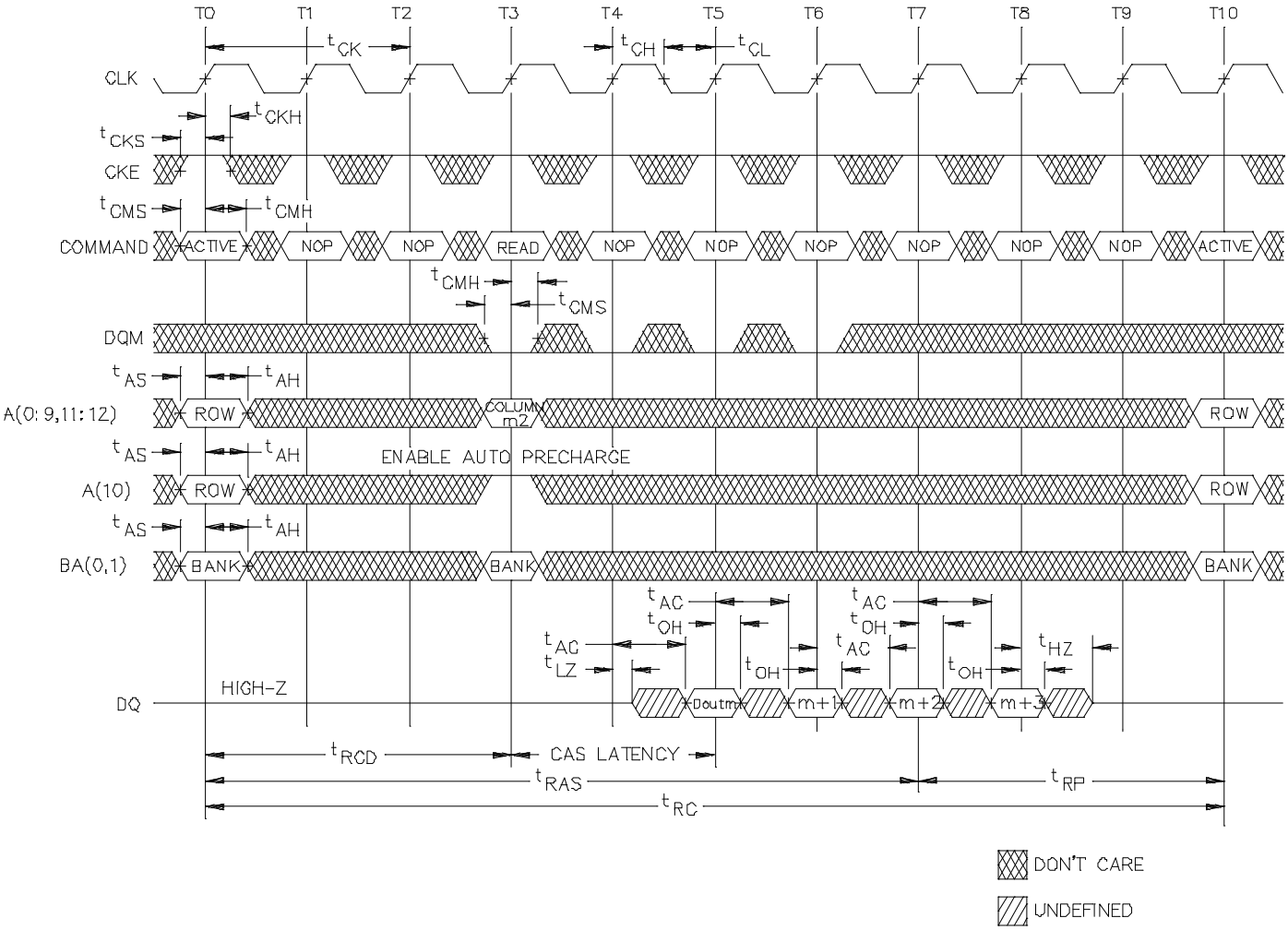
READ – without auto precharge



Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a “manual” PRECHARGE.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

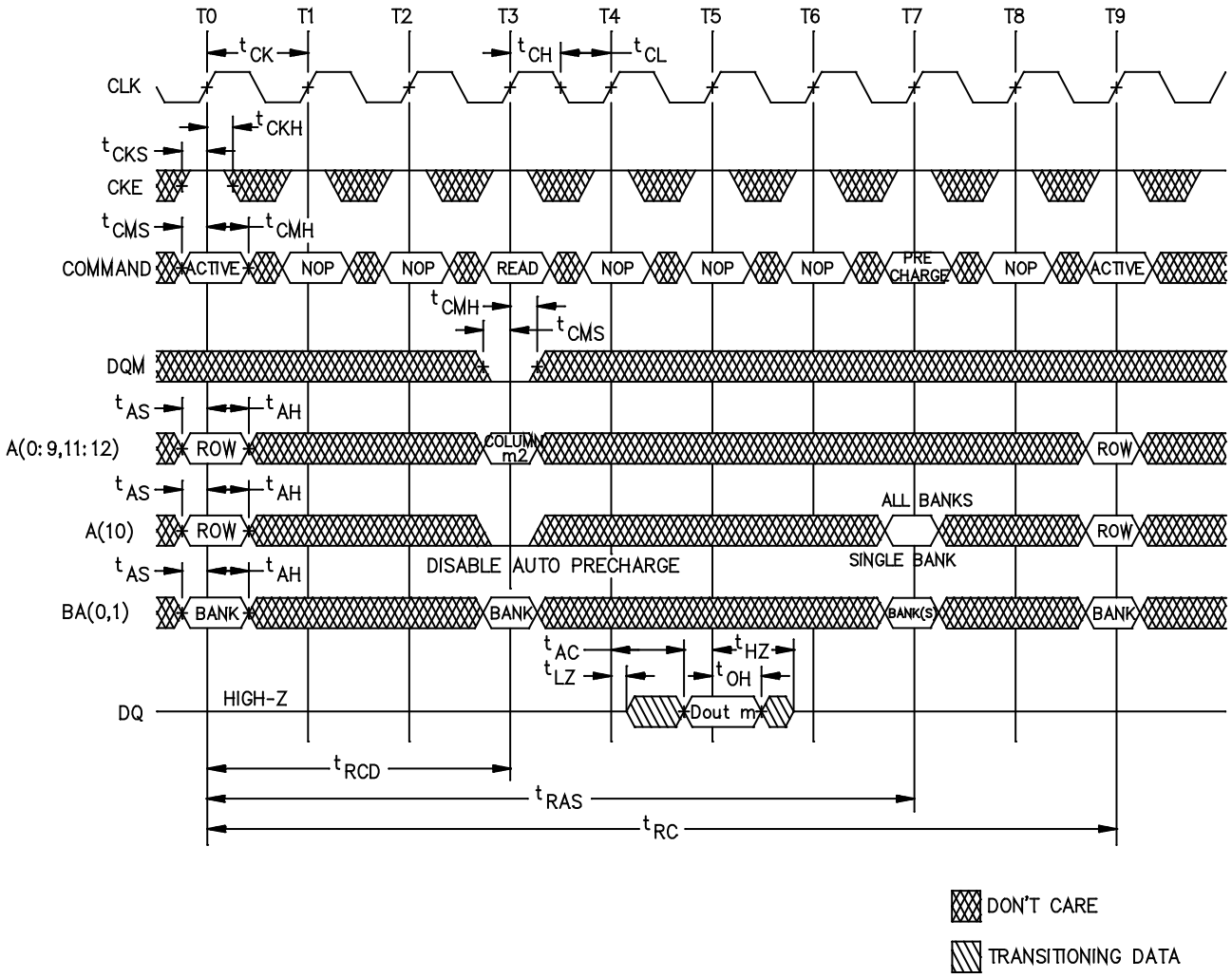
READ – with auto precharge



Notes: 1. For this example, BL = 4, and CL = 2.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

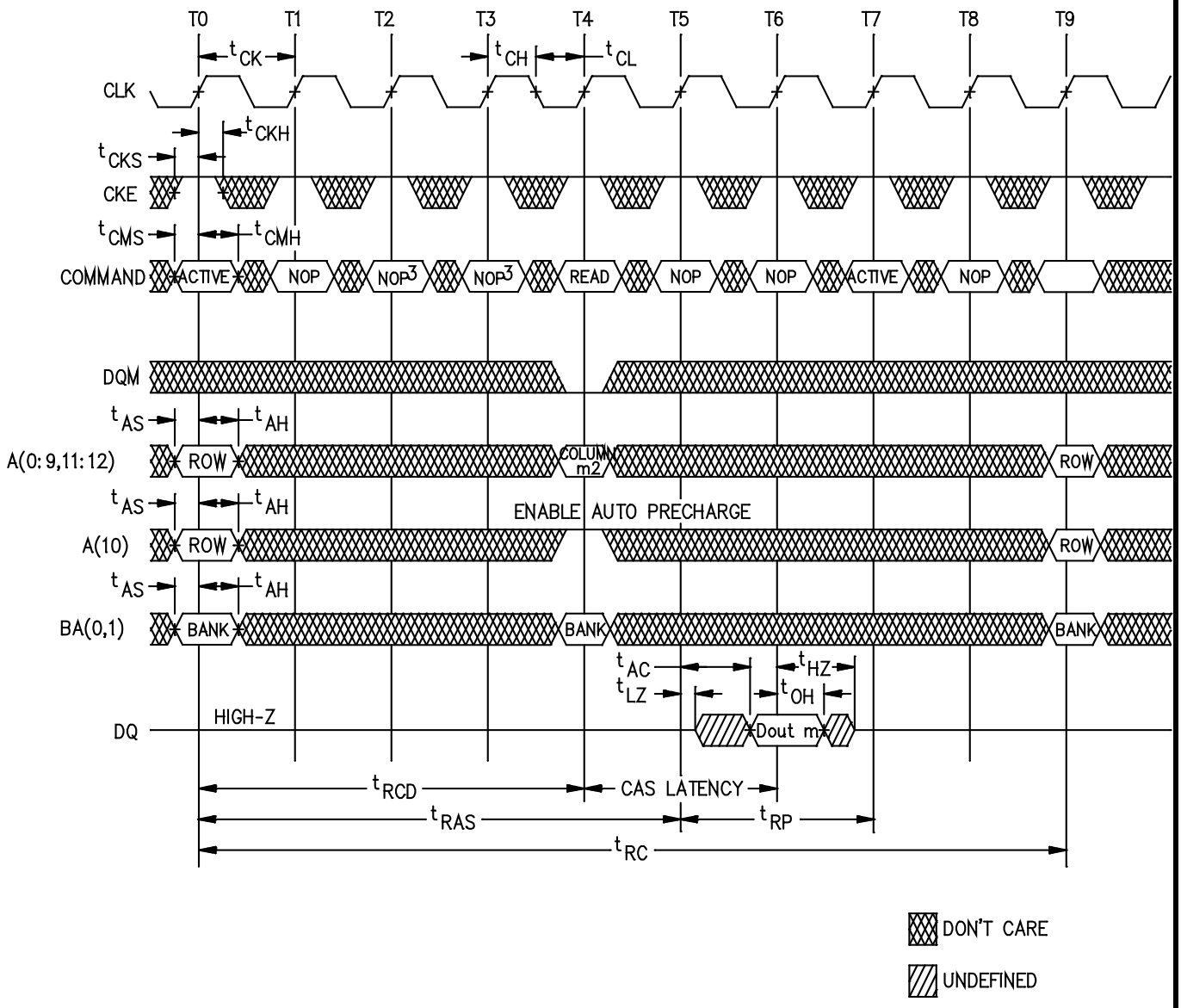
Single READ – without auto precharge



Notes: 1. For this example, BL = 1, and CL = 2 and the READ burst is followed by a manual PRECHARGE.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

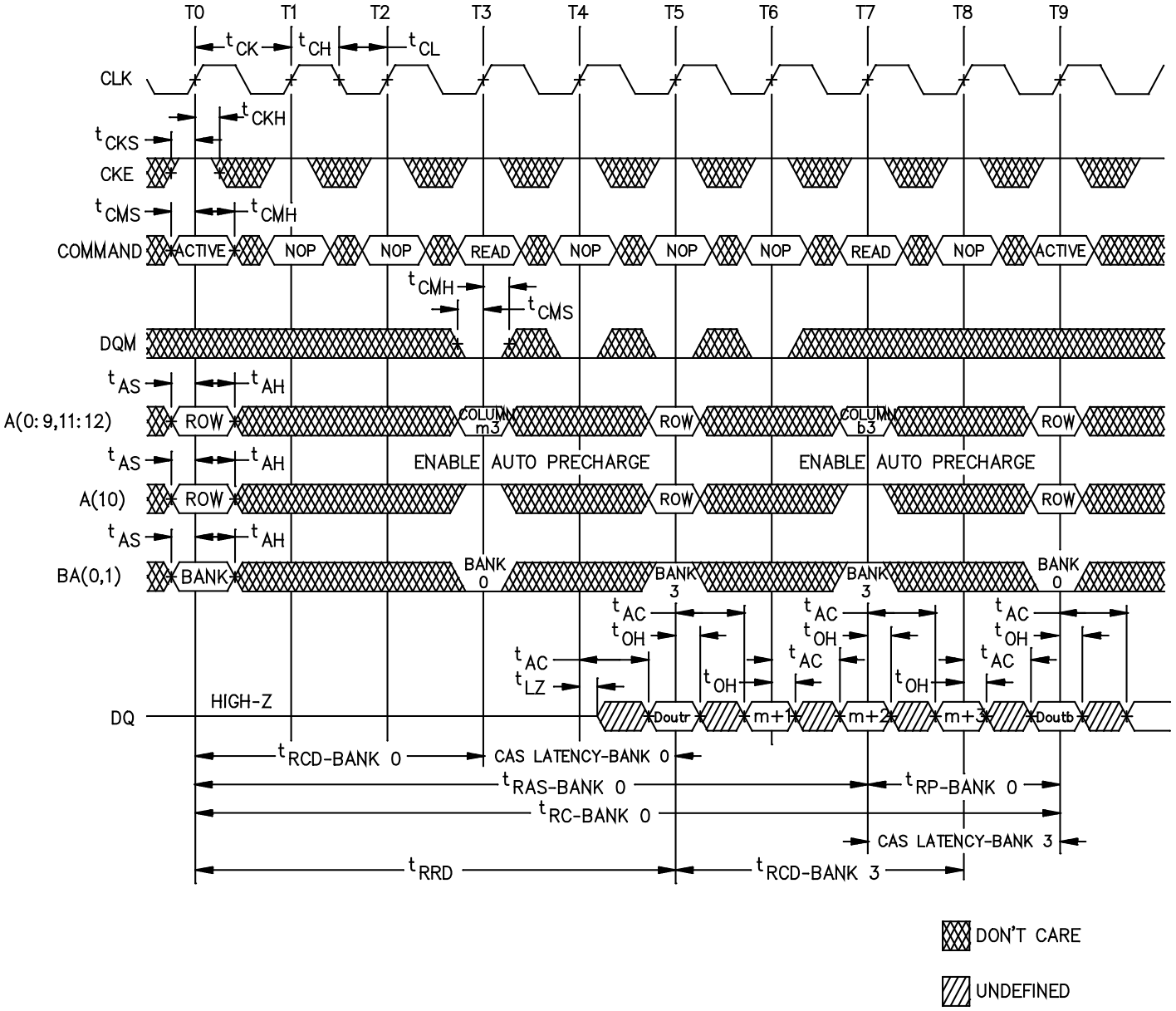
Single READ – with auto precharge



Notes: 1. For this example, BL = 1, and CL = 2.
2. A12 = “Don’t care”.
3. READ command not allowed (would violate t_{RAS}).

FIGURE 5. Timing waveforms - Continued.

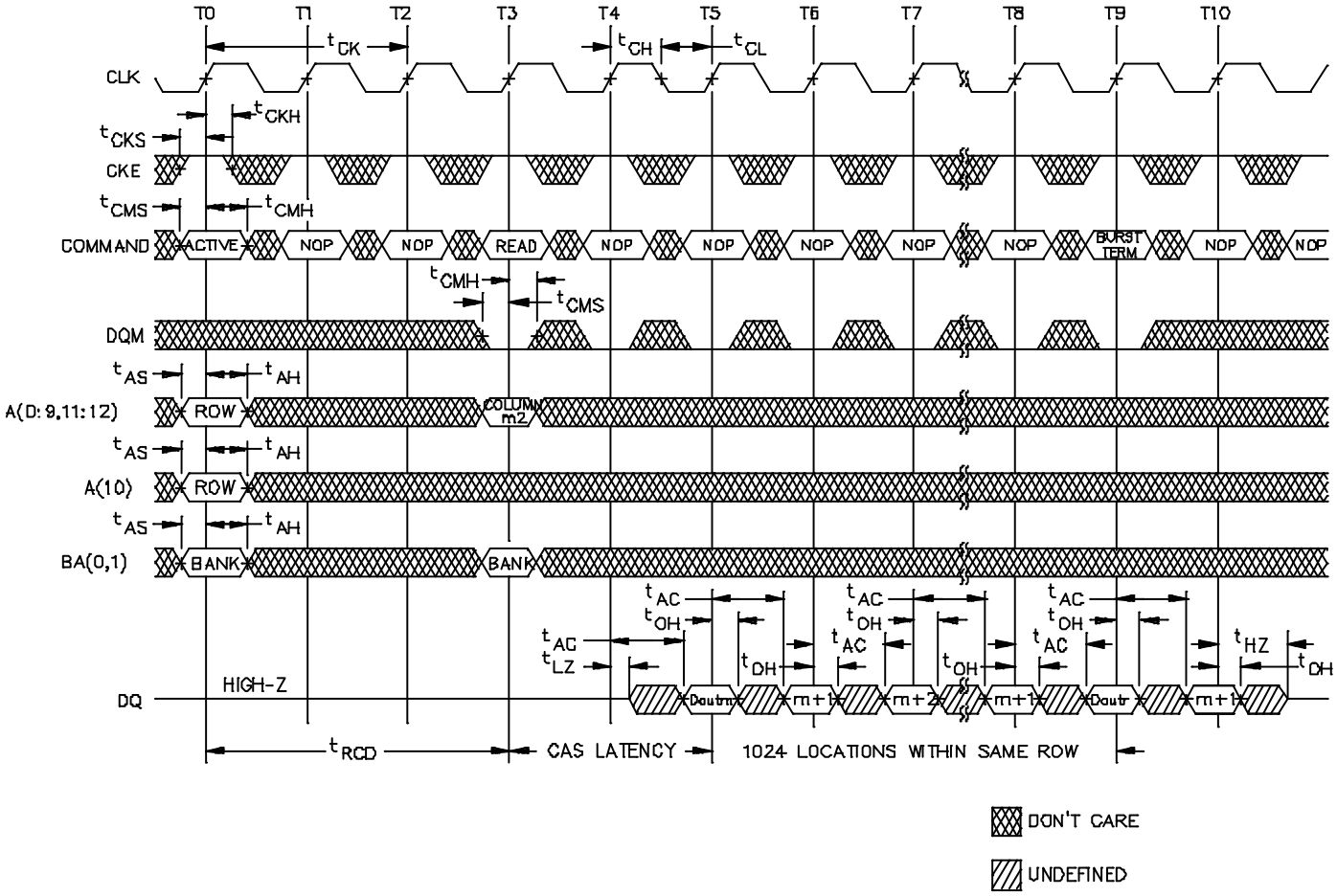
Alternating bank read accesses



Notes: 1. For this example, BL = 4, and CL = 2.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

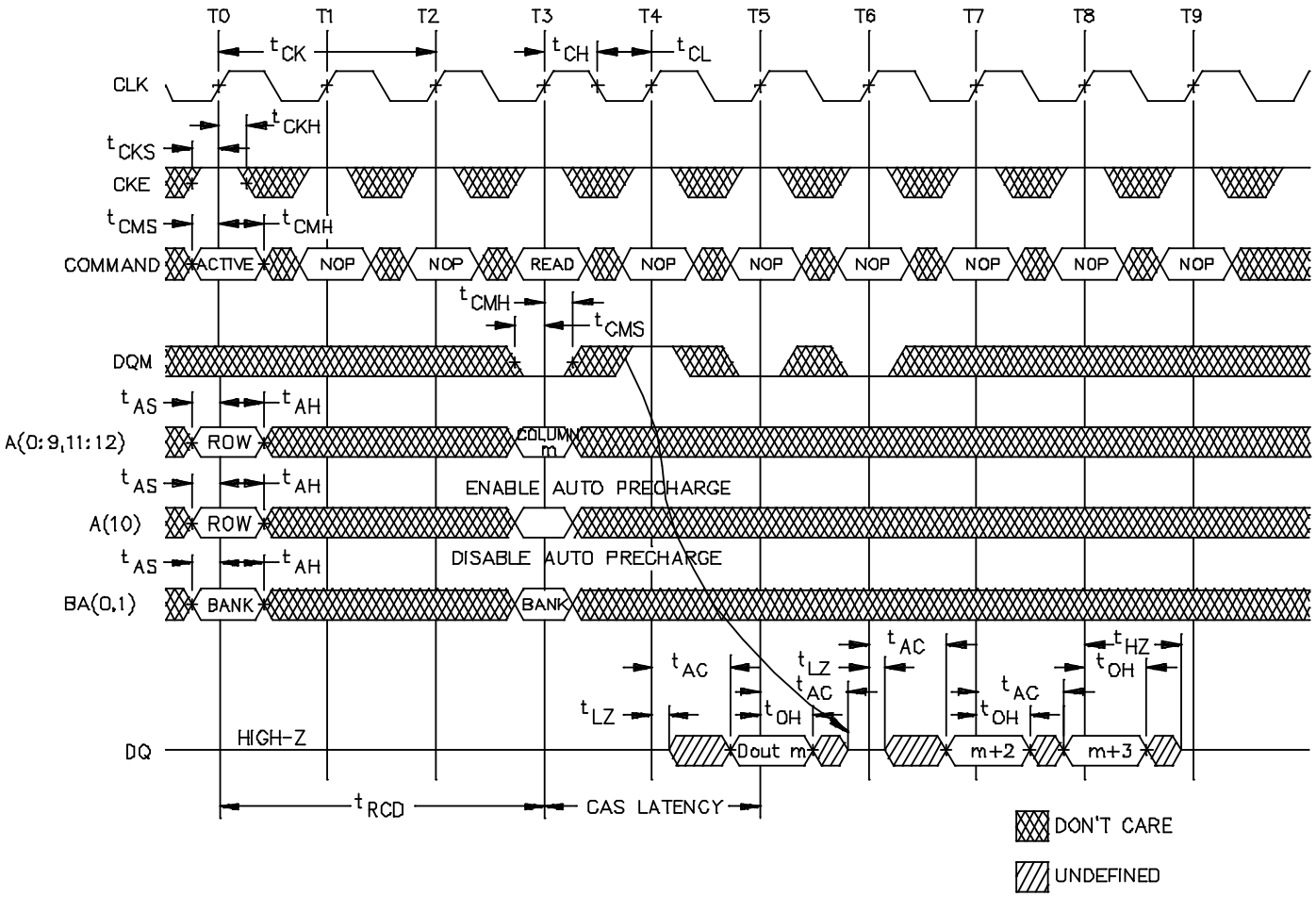
READ – full-page burst



Notes: 1. For this example, CL = 2.
2. A12 = “Don’t care”.
3. Page left open; no t_{RP}.

FIGURE 5. Timing waveforms - Continued.

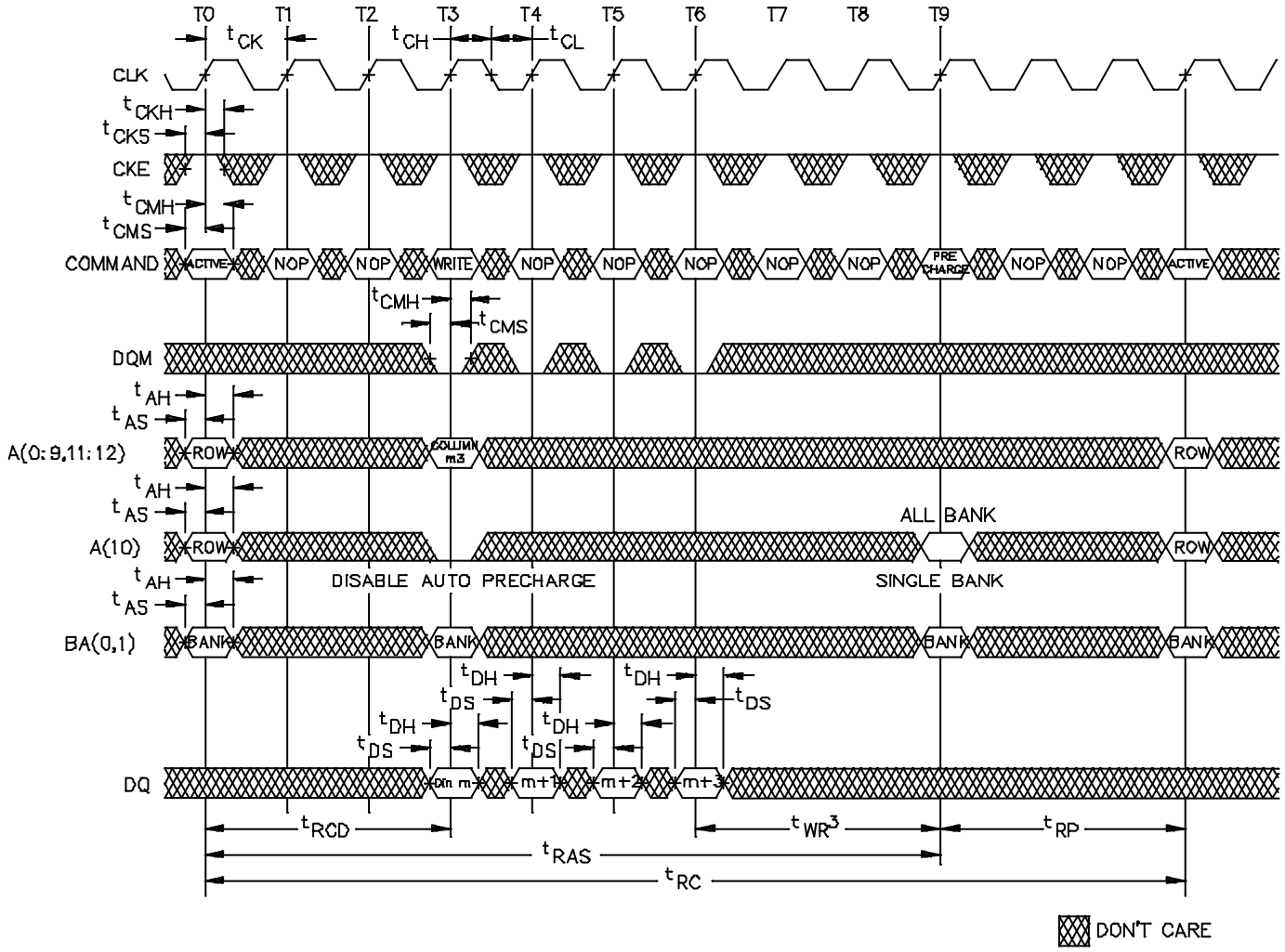
READ DQM operation



Notes: 1. For this example, BL = 4, and CL = 2.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

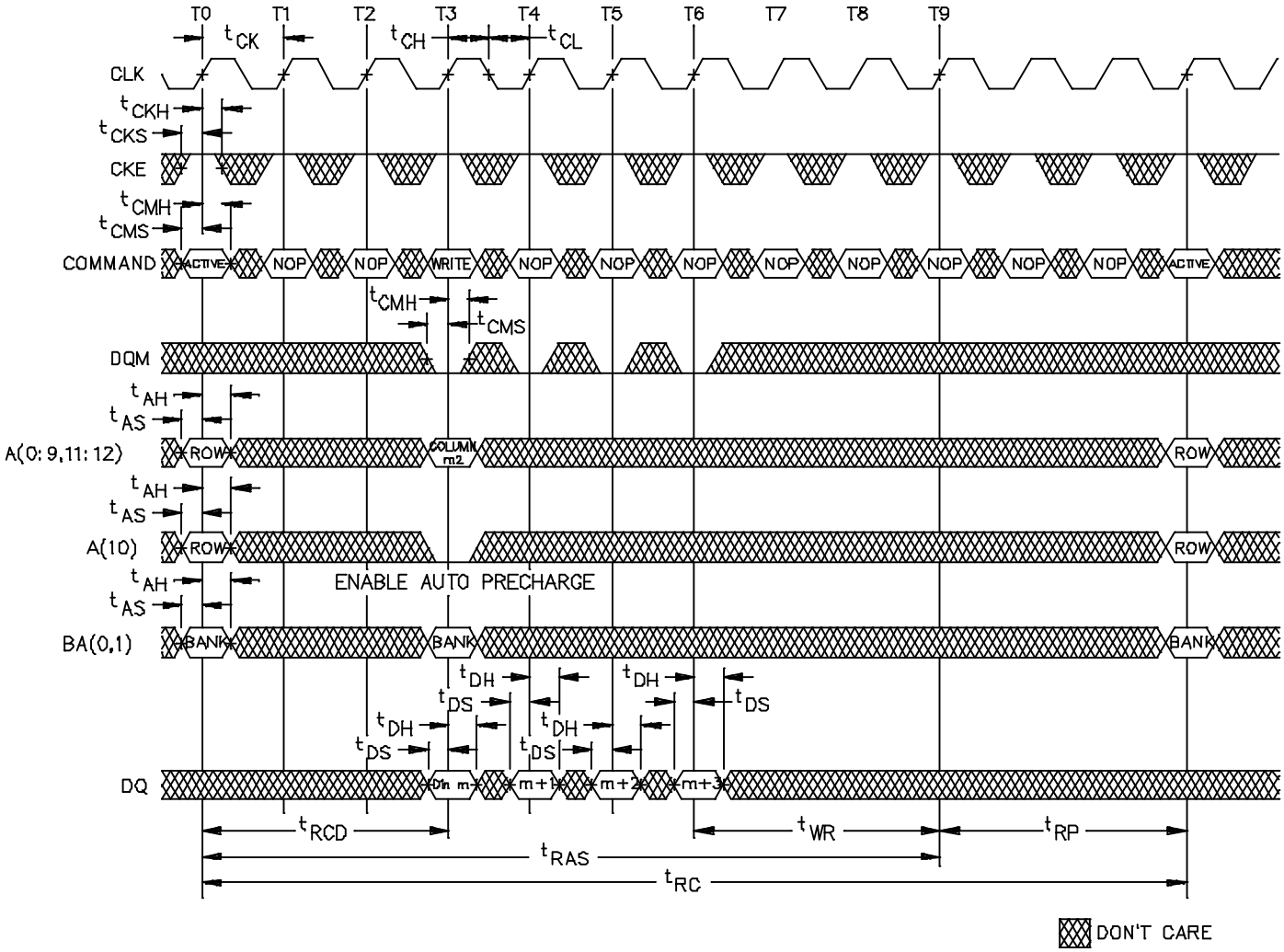
WRITE – without auto precharge



Notes: 1. For this example, BL = 4, and the WRITE burst is followed by a manual PRECHARGE.
2. 14 ns to 15 ns is required between <Din m+3> and the PRECHARGE command, regardless of frequency.
3. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

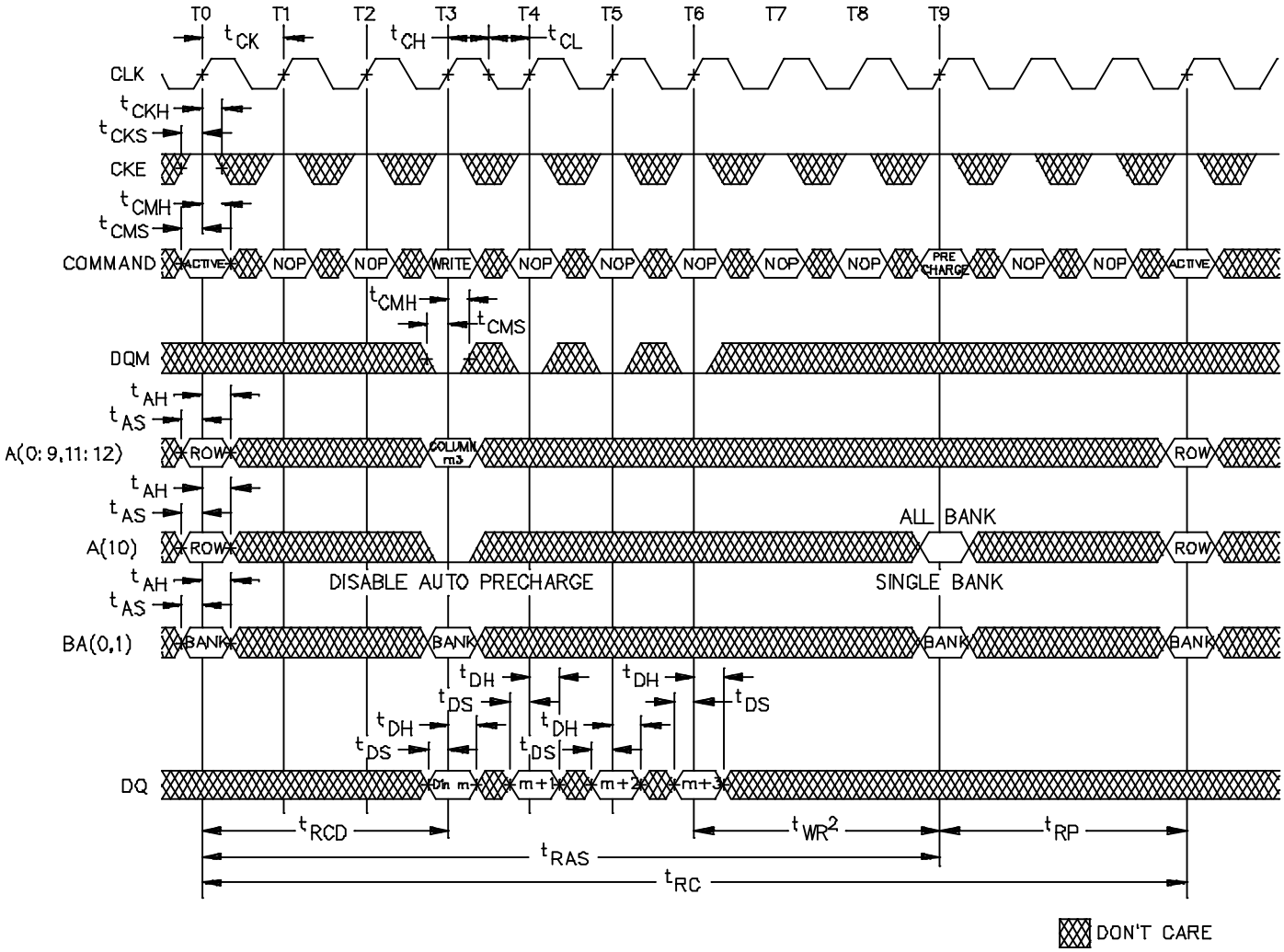
WRITE – with auto precharge



Notes: 1. For this example, BL = 4.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

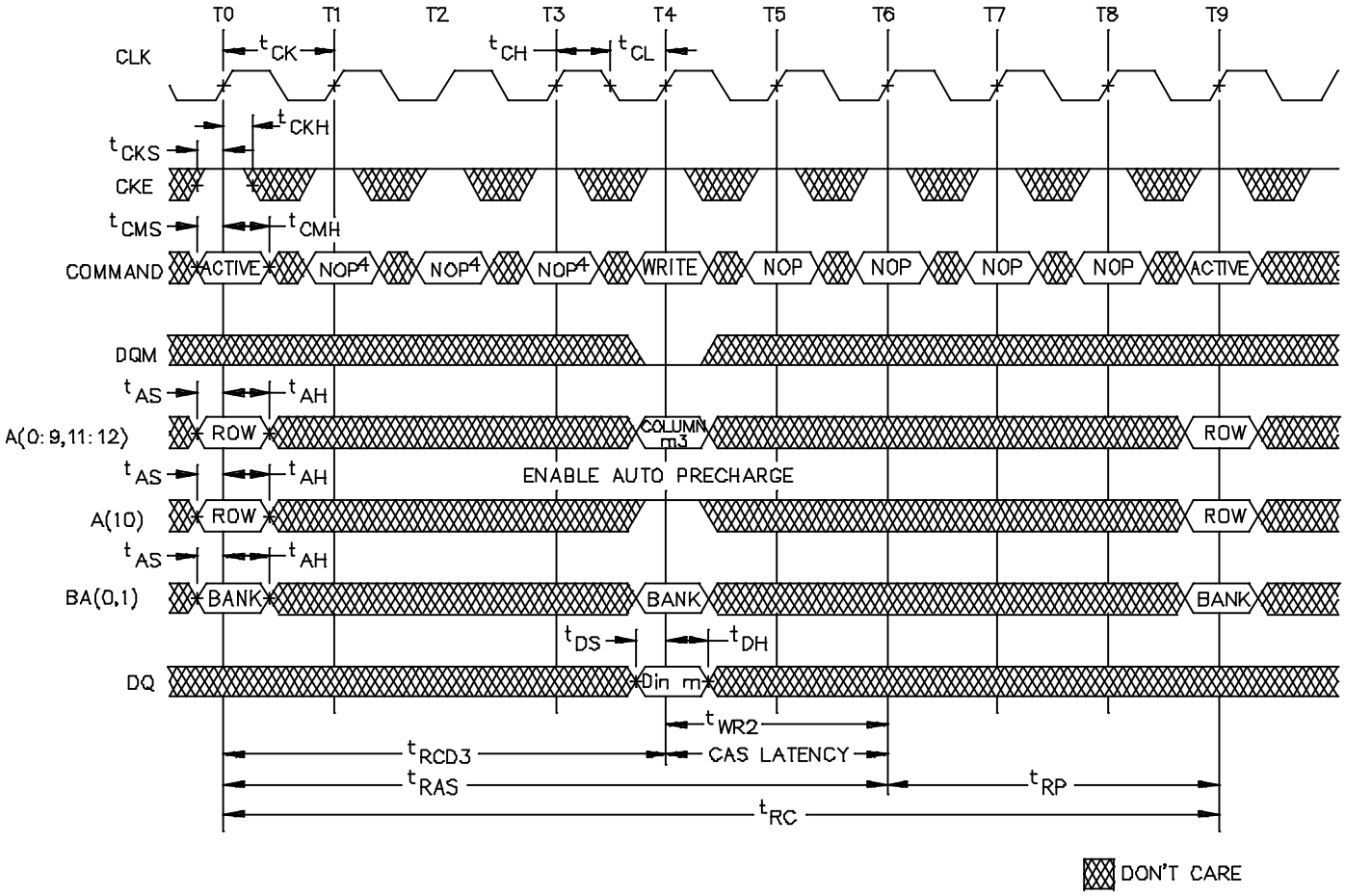
Single WRITE – without auto precharge



Notes: 1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE
2. 14 ns to 15 ns is required between <Din m> and the PRECHARGE command, regardless of frequency.
3. A12 = “Don’t care”.
4. PRECHARGE command not allowed else t_{RAS} would be violated.

FIGURE 5. Timing waveforms - Continued.

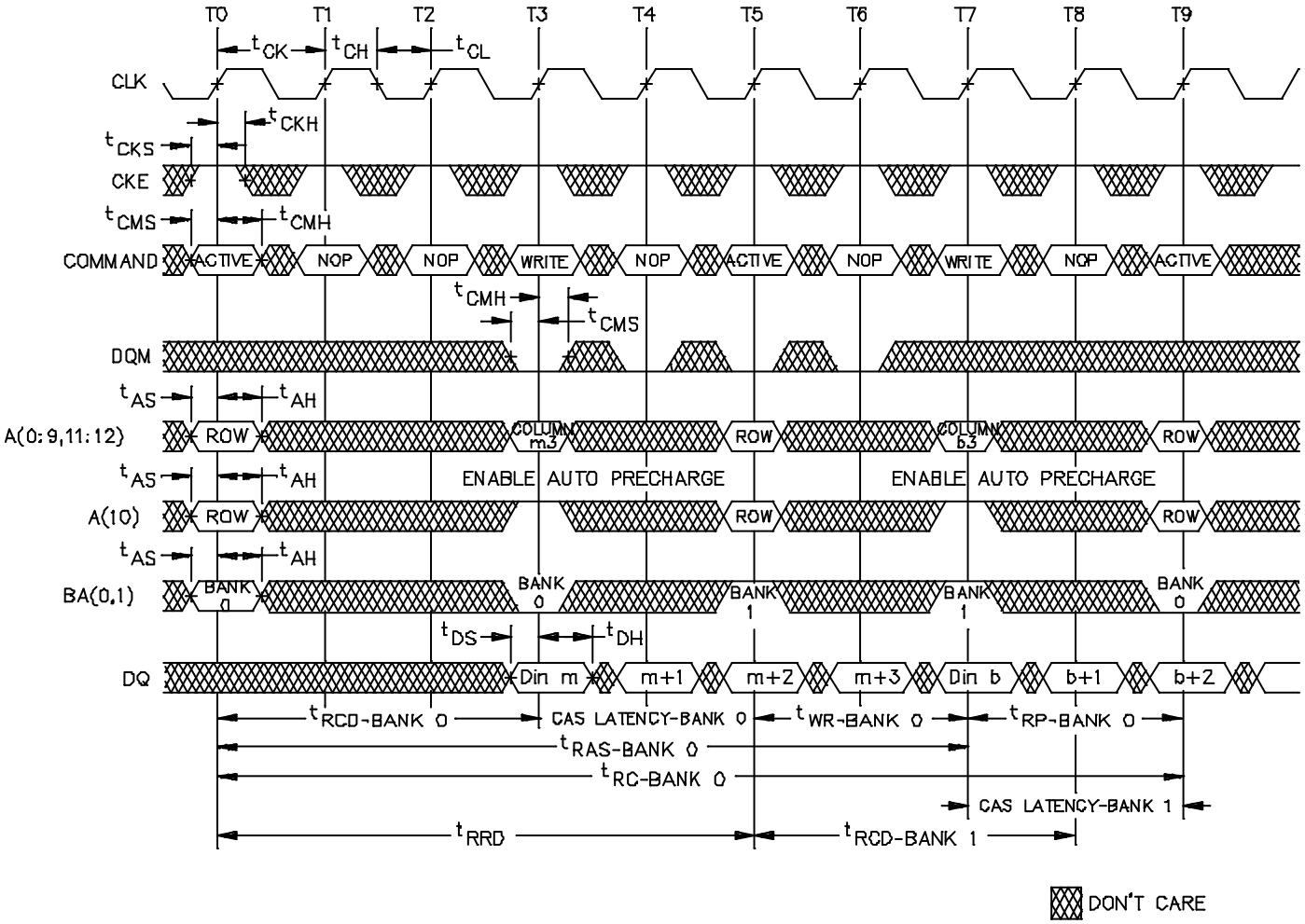
Single WRITE – with auto precharge



Notes: 1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE
2. 14 ns to 15 ns is required between <Din m> and the PRECHARGE command, regardless of frequency.
3. A12 = “Don’t care”.
4. PRECHARGE command not allowed (would violate t_{RAS})

FIGURE 5. Timing waveforms - Continued.

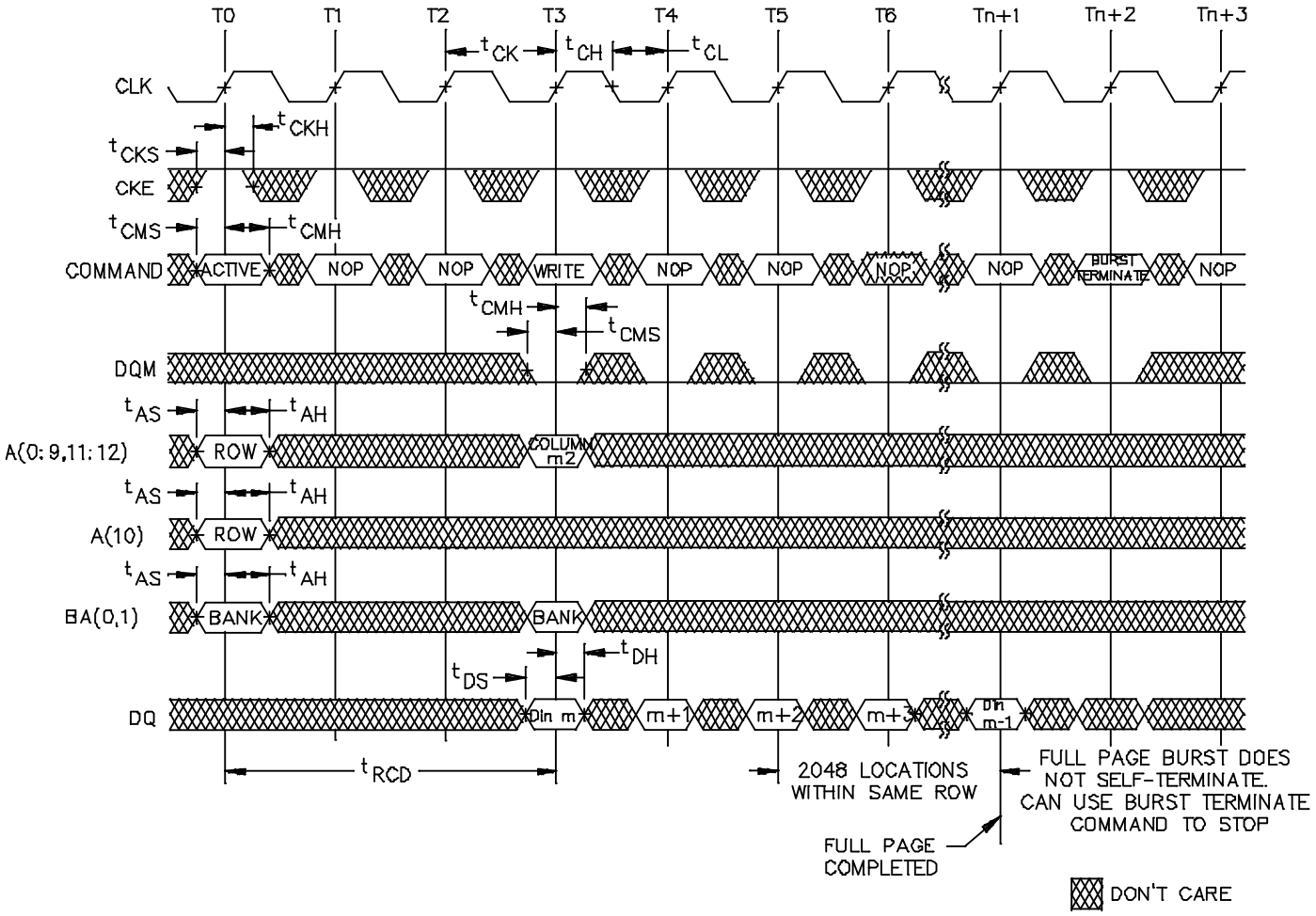
Alternating bank WRITE accesses



Notes: 1. For this example, BL = 4, CL = 2.
2. Requires one clock pulse time (10 ns) with auto precharge or 20 ns with PRECHARGE.
3. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

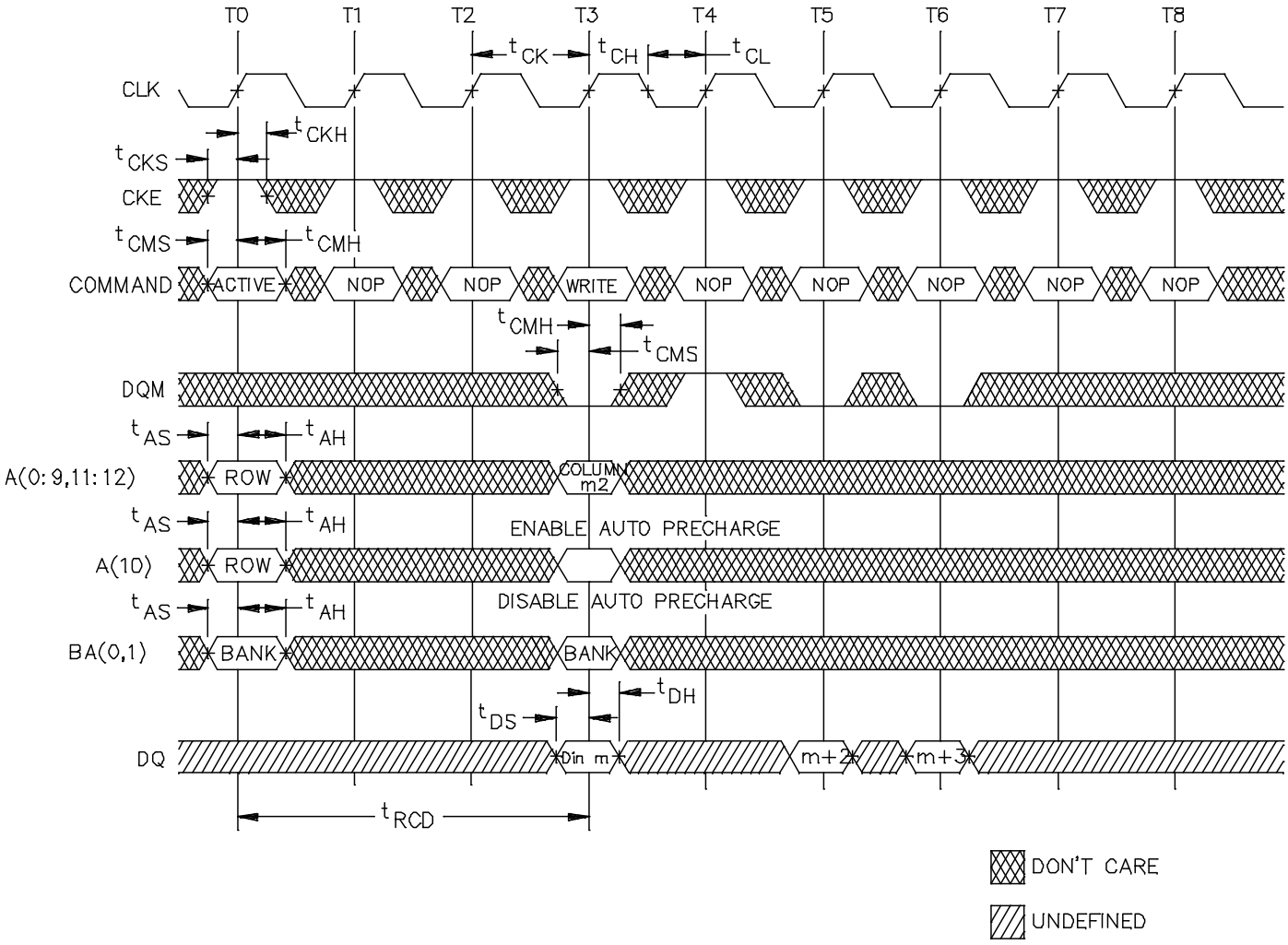
WRITE full-page burst



Notes: 1. A12 = “Don’t care”.
2. t_{WR} must be satisfied prior to PRECHARGE command.
3. Page left open; no t_{RP}.

FIGURE 5. Timing waveforms - Continued.

WRITE – DQM operation



Notes: 1. For this example, BL = 4.
2. A12 = “Don’t care”.

FIGURE 5. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in Table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

d. Additional screening for device type 02.

(1) 100% internal visual, method 2010 condition A of MIL-STD-883

(2) 100% PIND (Single pass).

(3) Serialization

(4) 100% X-ray (Top view only).

(5) Group A.

(6) Dynamic burn-in, deltas, PDA (3%) for Functional Test only, and PDA (10%) for DC and Functional Test combined.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in Table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (Latch up) tests shall be measured only for the initial qualification and after any process or design changes which may affect the performance of the device. For device classes Q and V, the procedures and circuit shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard Number 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535 and the end-point electrical parameters shall be as specified in Table IIA herein.

a. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in Table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in Table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A, and as specified herein. The total dose requirements shall be as defined within paragraph 1.5 herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in Table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C $\pm$5ºC. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º $\leq$ angle $\leq$ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. The fluence shall be $\geq$ 100 errors or $\geq 10^6$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 microns in silicon.

e. The test temperature shall be +25ºC ±10ºC for single event upset testing and at the maximum rated operating temperature $\pm$10ºC for single event upset testing.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	- - -	1*,2,3,7*,8A, 8B,9,10,11
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1	- - -	1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	- - -	1*, 7* Δ
6	Final electrical parameters	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*,8A, 8B,9,10,11
7	Group A test requirements	1,2,3,4**,7, 8A,8B,9,10,11	1,2,3,4**,7,8A, 8B,9,10,11
8	Group C end-point electrical parameters	2,3,7,8A,8B	1,2,3,7,8A,8B, 9,10,11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9

1/ Blank spaces indicates tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify functionality of the device.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to previous interim electrical parameters (see Line 1). For device class V, performance of delta limits shall be specified in the manufacturer's QM plan..
7/ See 4.4.1d.

Table IIB. Delta limits at +25ºC.

Parameter 1/	Limit	Unit
Supply current standby at 0 MHz I_{DD2}	± 10% of specified value in Table IA	mA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614)692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-03-26

Approved sources of supply for SMD 5962-10230 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R1023001QXC	65342	UT8SDMQ64M48-75YEC
5962R1023001QYC	65342	UT8SDMQ64M48-75ZEC
5962R1023002QXC	65342	UT8SDMQ64M48-75YEC
5962R1023002QYC	65342	UT8SDMQ64M48-75ZEC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs, Inc. 4350 Centennial Blvd. Colorado Springs, CO 80907-7370